

## Evaluating the **ADRV9008-1** Direct Conversion Receiver and the **ADRV9008-2** and **ADRV9009** Direct Conversion Transceivers

### OVERVIEW

The [ADRV9008-1](#), [ADRV9008-2](#), and [ADRV9009](#) demonstration system allows customers to evaluate a device without developing custom software or hardware. The system is comprised of a radio daughter card, a Zynq® motherboard from Analog Devices, Inc., an SD card with an operating system, two power supplies, and a C#-based evaluation software application. The evaluation system uses an Ethernet interface to communicate with the PC.

### INITIAL SETUP

The [ADRV9008-1](#), [ADRV9008-2](#), and [ADRV9009](#) transceiver evaluation software (TES) can run with or without evaluation hardware. When the TES runs without the hardware connected, the software can be fully configured for a particular operating mode. If the evaluation hardware is connected, the desired operating parameters can be set up with the TES. Then, the software can program the [ADRV9008-1](#), [ADRV9008-2](#), and [ADRV9009](#) evaluation hardware. After the device is configured, the evaluation software can be used to transmit waveforms, observe received waveforms, and initiate correction algorithms. An initialization sequence in the form of an IronPython script can be generated and executed using the TES.

### HARDWARE KIT

The [ADRV9008-1](#), [ADRV9008-2](#), and [ADRV9009](#) demonstration system kit contains the [ADRV9008-1](#), [ADRV9008-2](#), and [ADRV9009](#) evaluation board in the form of a daughter card with a field programmable gate array (FPGA) mezzanine card (FMC) connector, one 6 V/2 A switching power supply, and one SD card containing an image of a Linux® operating system with the required evaluation software. The SD card type is 8 GB size, Type 4.

### HARDWARE AND SOFTWARE REQUIREMENTS

The hardware and software requirements are as follows:

- The Zynq evaluation platform (Analog Devices, BVAL-TPG-ZYNQ3, Revision 1.2. This evaluation platform is not included in the [ADRV9008-1](#), [ADRV9008-2](#), and [ADRV9009](#) demonstration kit.
- The [ADRV9008-1](#), [ADRV9008-2](#), and [ADRV9009](#) demonstration system kit.
- The operating system on the controlling PC must be Windows® 7 (x86 and x64) or Windows 8 (x86 and x64).
- The PC must have an open Ethernet port with the following constraints:
  - If the Ethernet port is occupied by another LAN connection, a USB to Ethernet adapter can be used.
  - The PC must be able to access the following ports over this dedicated Ethernet connection:
    - 22—secure shell (SSH) protocol.
    - 55555—access to the evaluation software on the Zynq platform.
- TES available from the [design center landing page](#).
- The user must have administrative privileges. To run software automatic updates, the PC must have access to the internet. If internet access is restricted, perform a manual software update.

### HARDWARE SETUP

The Zynq platform setup requires the following procedure:

1. Ensure that all jumpers are in the positions shown in Figure 1.
2. SW11 must be in the positions shown in Figure 1 (Slider 1, Slider 2, and Slider 5 are in the A position).
3. The SD card included with the evaluation kit must be placed in the J30 slot of the Zynq platform.

The evaluation hardware setup is shown in Figure 2, Figure 3, and Figure 4.

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## REVISION HISTORY

6/2018—Revision 0: Initial Version

## EVALUATION BOARD PHOTOGRAPHS

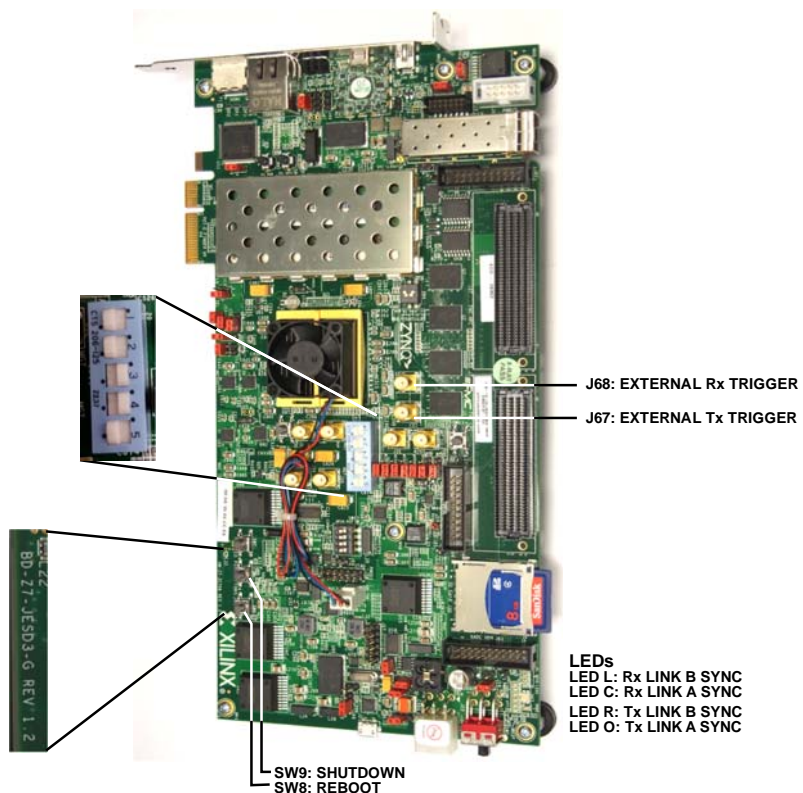


Figure 1. Zynq Evaluation Board with Jumper Settings and Switch Positions Configured to Work with the ADRV9008-1, ADRV9008-2, and ADRV9009 Evaluation Board

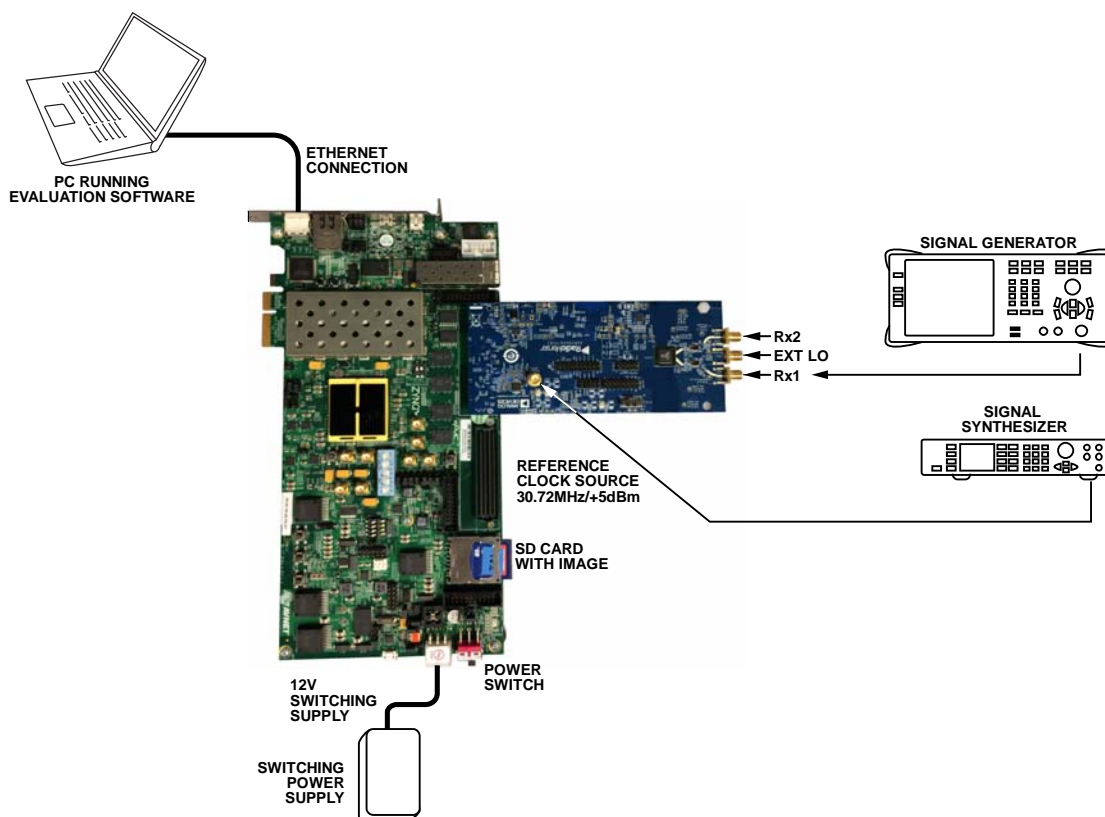


Figure 2. ADRV9008-1 Receiver Evaluation Board and Zynq Motherboard with Connections Required for Receiver 1 Testing

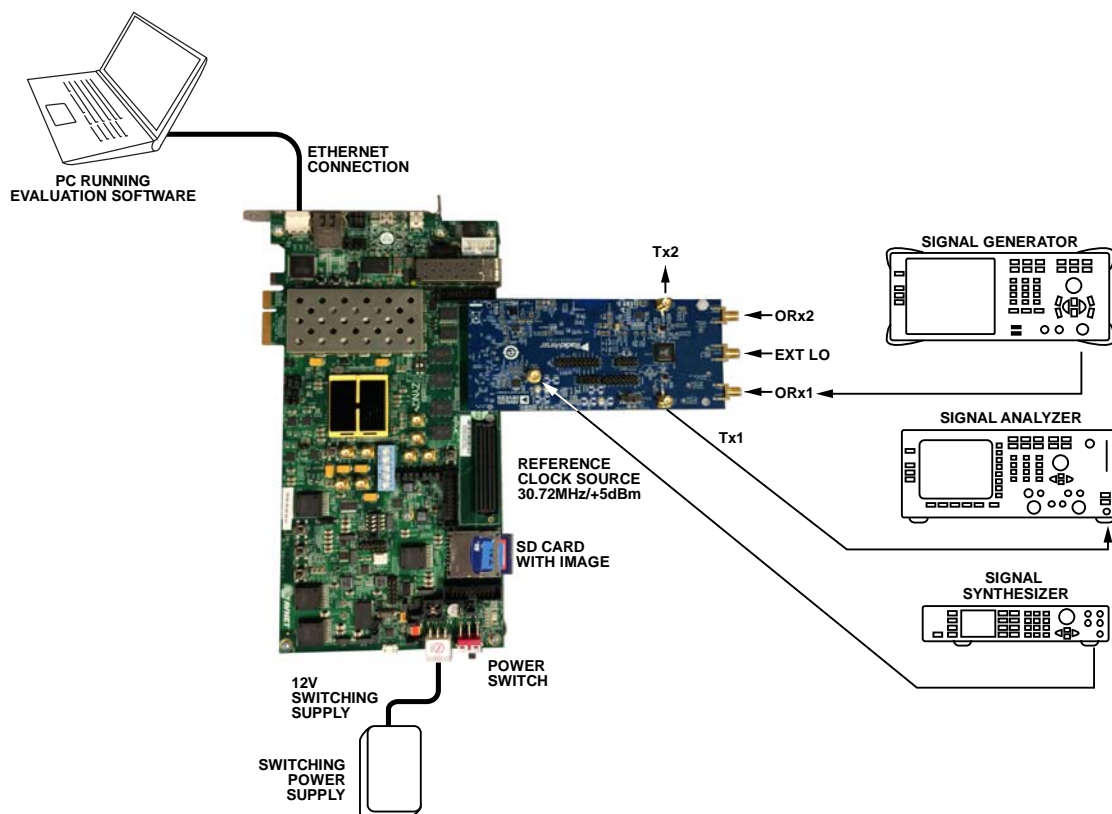


Figure 3. ADRV9008-2 Transmitter Evaluation Board and Zynq Motherboard with Connections Required for Transmitter 2 and Observation Receiver 1 Testing

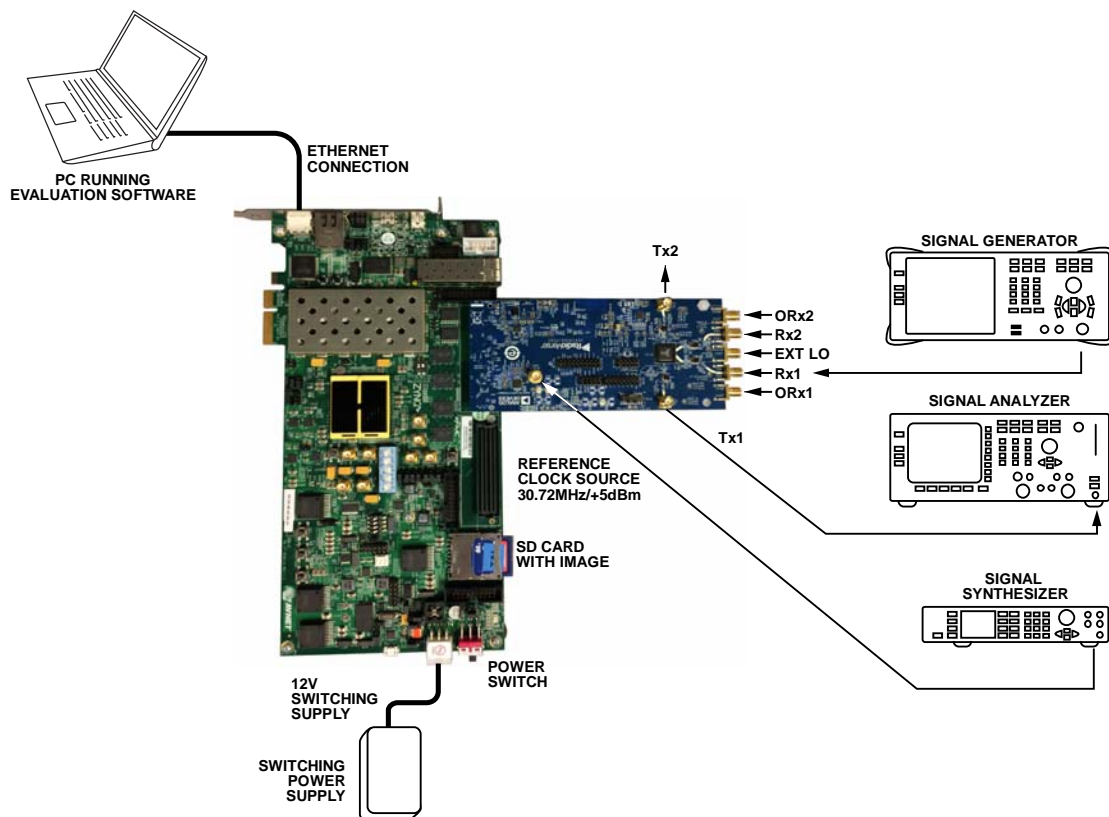


Figure 4. ADRV9009 Time Division Duplex (TDD) Evaluation Board and Zynq Motherboard with Connections Required for Transmitter 2 and Receiver 1 Testing

## SETTING UP THE EVALUATION BOARD

To set up the evaluation board for testing, use the following procedure:

1. Connect the [ADRV9008-1](#), [ADRV9008-2](#), and [ADRV9009](#) evaluation board and the Zynq evaluation platform together as shown in Figure 2, Figure 3, or in Figure 4. Use the high pin count (HPC) FMC connector (J37). Ensure that the connectors are properly aligned.
2. Ensure that all jumpers on the Zynq motherboard, as well as the SW11 position, match the settings shown in Figure 1 (Slider 1, Slider 2, and Slider 5 are in the A position).
3. Insert the SD card included with the [ADRV9008-1](#), [ADRV9008-2](#), and [ADRV9009](#) evaluation kit into the Zynq SD card slot (J30).
4. On the [ADRV9008-1](#), [ADRV9008-2](#), and [ADRV9009](#) evaluation card, provide a 30.72 MHz clock source (or frequency match the setting selected on the [AD9528](#) configuration tab, shown in Figure 31), at a 5 dBm power level to the J401 connector. This signal drives the reference clock into the [AD9528](#) clock generation chip on the board. The REFA pin and the  $\overline{\text{REFA}}$  pin of the [AD9528](#) generate the device clock for the [ADRV9008-1](#), [ADRV9008-2](#), and [ADRV9009](#), and the REF\_CLK for the FPGA on the Zynq platform.
5. Connect a 6 V, 2 A power supply, such as the HF-FYD FY0602000 (supplied), to the [ADRV9008-1](#), [ADRV9008-2](#), and [ADRV9009](#) evaluation board at the P501 header.
6. Connect a 12 V, 5 A power supply to the Zynq evaluation platform at the J22 header.
7. Connect the Zynq evaluation platform to the PC with an Ethernet cable, connected to P3. There is no driver installation required.
  - a. In a case where the Ethernet port is already occupied by another connection, use an USB to Ethernet adapter.
  - b. On an Ethernet connection dedicated to the Zynq platform, the user must manually set the IPv4 address to 192.168.1.2 and the IPv4 subnet mask to 255.255.255.0

See Figure 5 for more details. Ensure that the following ports are not blocked by firewall software on the PC:

- 22—SSH protocol.
- 55555—access to the evaluation software on the Zynq platform.

The Zynq IP address is set by default to 192.168.1.10.

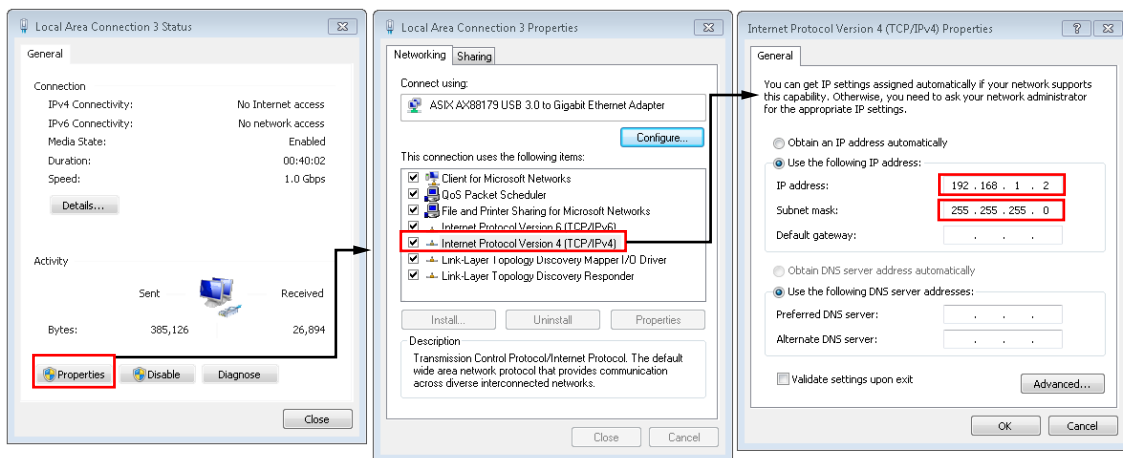


Figure 5. IP Settings for the Ethernet Port Dedicated to the Zynq Platform

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## HARDWARE SETUP AND OPERATION

### HARDWARE SETUP FOR EXTERNAL TRANSMITTER LO LEAKAGE CALIBRATION

The [ADRV9008-1](#), [ADRV9008-2](#), and [ADRV9009](#) are direct conversion transceivers. One drawback of the direct conversion technique is that the transmitter baseband dc offset and direct coupling of the local oscillator to the transmitter output can cause an undesired continuous wave (CW) emission at the transmitter local oscillator (LO) frequency. The purpose of the transmitter LO leakage (LOL) calibration is to minimize this CW emission. The [ADRV9008-1](#), [ADRV9008-2](#), and [ADRV9009](#) evaluation system supports two types of transmitter LOL calibration algorithms. The user can select calibration algorithms using the tick boxes shown in the Figure 20.

When the user selects internal calibration algorithms LOL initialization calibration, no external hardware is necessary. In this case, there is no transmitter LOL tracking calibration available.

When the user selects external transmitter LOL initialization calibration and external transmitter LOL tracking calibration, the LOL tracking calibration runs on the evaluation system. For proper operation, external components must be connected to the [ADRV9008-1](#), [ADRV9008-2](#), and [ADRV9009](#) evaluation platform. Figure 6 and Figure 7 show the correct configuration to demonstrate the performance of the transmitter LOL

calibration algorithm. The user must connect a radio frequency (RF) splitter at the trans-mitter output. One of the splitter outputs must be connected to the corresponding [ADRV9008-1](#), [ADRV9008-2](#), and [ADRV9009](#) observation receiver inputs through an RF attenuator (Transmitter 1, Observation Receiver 1, Transmitter 2, then Observation Receiver 2). The amount of attenuation required depends on the attenuation introduced by the splitter. For maximum observation receiver gain, the signal level at the observation receiver input must not exceed  $-16$  dBm.

For external transmitter LOL tracking calibration, both transmitters must be looped back to both observation receivers through splitters and attenuators. For the best LOL performance when operating above 4 GHz, use only the Observation Receiver 1 input for both Transmitter 1 and Transmitter 2. Use an external switch to accomplish this configuration.

Use the following example settings to determine the RF attenuator specification:

- Transmitter output signal = 7 dBm (CW)
- Maximum observation receiver gain
- RF splitter attenuation = 3 dB
- Maximum observation receiver input =  $-16$  dBm
- RF attenuator = 20 dB ( $7 \text{ dBm} - 3 \text{ dB} - 20 \text{ dB} = -16 \text{ dBm}$ )

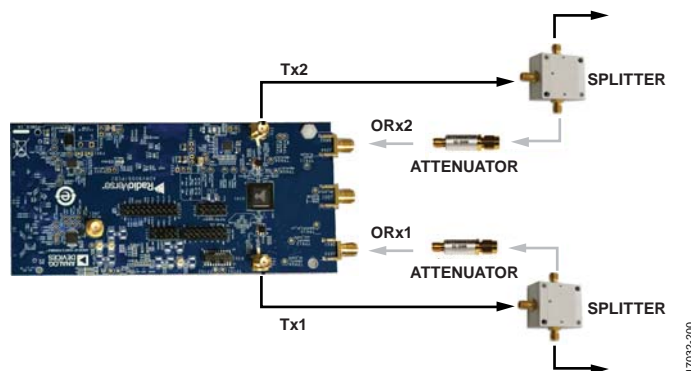


Figure 6. Demonstration Operation of External Transmitter LOL Calibration on the [ADRV9008-2](#) Transmitter and the Frequency Division Duplex (FDD) Evaluation System

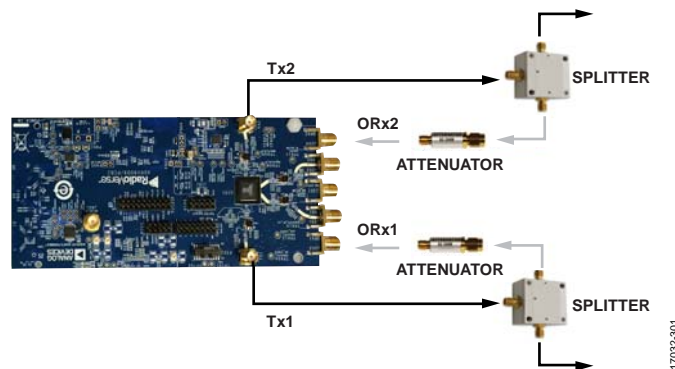


Figure 7. Demonstration Operation of External Transmitter LOL Calibration on the [ADRV9009](#) Transmitter and the TDD Evaluation System



Figure 8 and Figure 9 show the configuration in which the customer uses the [ADRV9008-1](#), [ADRV9008-2](#), and [ADRV9009](#) evaluation system with a desired power amplifier (PA). In this case, split or couple the signal after the PA to the corresponding observation receiver channel through an appropriate attenuator. The maximum signal level at the observation receiver input must not exceed  $-16$  dBm. The amount of attenuation required must be calculated based on the power level after the PA and RF coupler.

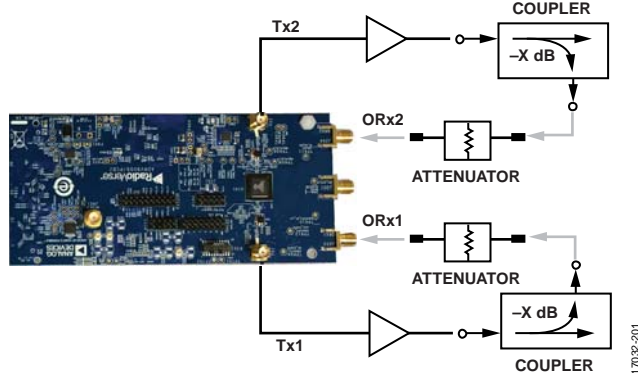


Figure 8. End User Application of External Transmitter LOL Calibration (Nonstitching Mode) Using the [ADRV9008-2](#) Transmitter and the FDD Evaluation System

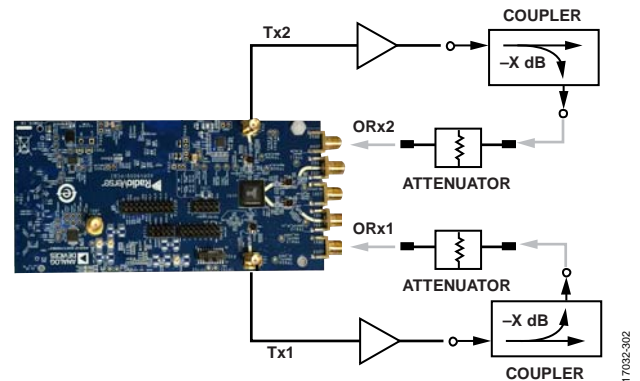


Figure 9. End User Application of External Transmitter LOL Calibration (Nonstitching Mode) Using the [ADRV9009](#) Transmitter and the TDD Evaluation System

The setup shown in Figure 8 and Figure 9 is used when nonstitching mode is used. When stitching mode is used (the observation receiver bandwidth  $> 200$  MHz), use the setup shown in Figure 10 and Figure 11.

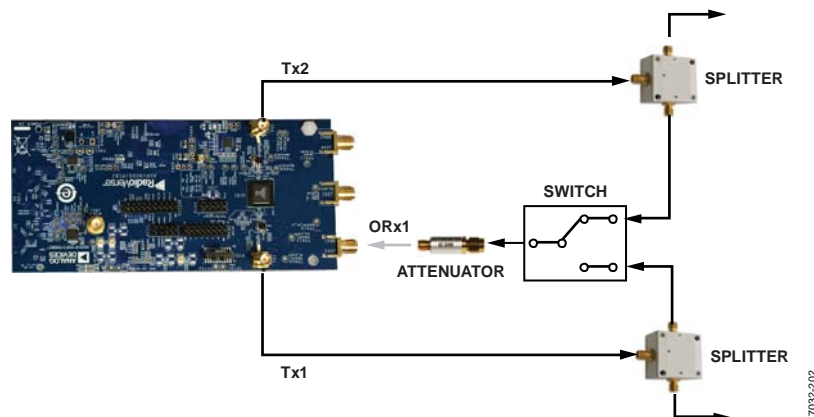


Figure 10. Demonstration Operation of the External Transmitter LOL Calibration (Stitching Mode) on the [ADRV9008-2](#) Transmitter and the FDD Evaluation System

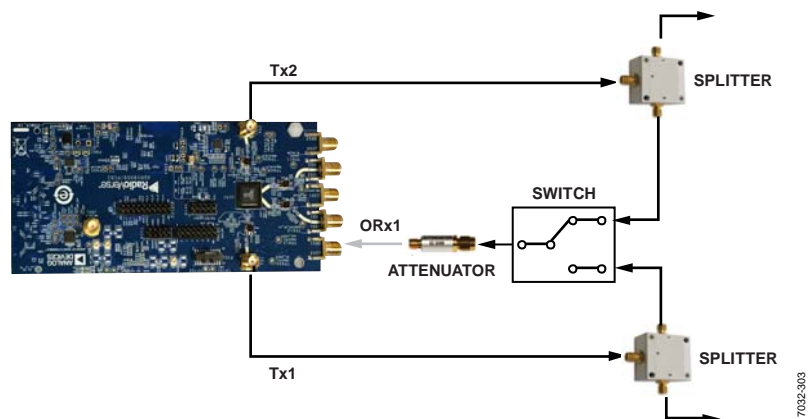


Figure 11. Demonstration Operation of the External Transmitter LOL Calibration (Stitching Mode) on the [ADRV9009](#) TDD Evaluation System

Figure 12 and Figure 13 show the configuration in which the customer uses ADRV9008-1, ADRV9008-2, and ADRV9009 evaluation system with a desired PA in stitching mode. In this case, split or couple the signal after the PA to the selected observation receiver channel. Observation Receiver 1 is selected

in Figure 12 and Figure 13 through an appropriate attenuator and a switch. The maximum signal level at the observation receiver input must not exceed  $-16$  dBm. The amount of attenuation required must be calculated based on the power level after the PA and the RF coupler.

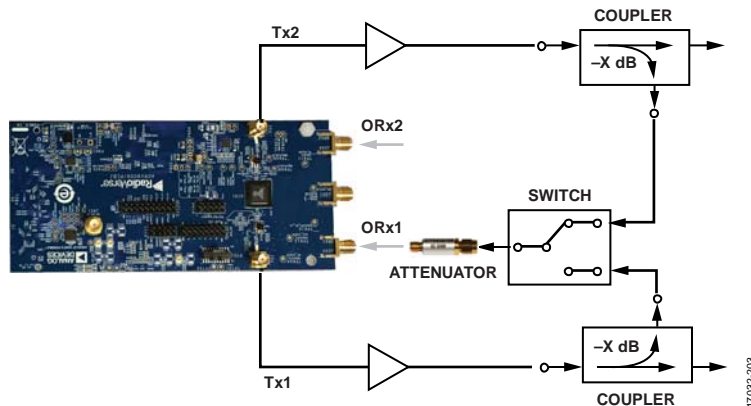


Figure 12. End User Application of External Transmitter LOL Calibration (Stitching Mode) Using the ADRV9008-2 Transmitter and the FDD Evaluation System

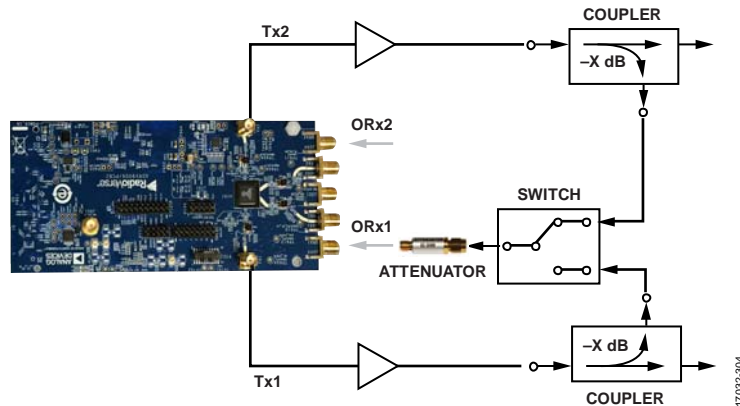


Figure 13. End User Application of External Transmitter LOL Calibration (Stitching Mode) Using the ADRV9009 Transmitter and the TDD Evaluation System



## HARDWARE OPERATION

For correct operation of the hardware, use the following procedure:

1. Turn on the evaluation system by switching the Zynq board power switch (SW1) to the on position. If the hardware is connected correctly, two green light emitting diodes (LEDs) on the [ADRV9008-1](#), [ADRV9008-2](#), and [ADRV9009](#) evaluation board, D501 and D502, are on.
2. The Zynq evaluation system uses a Linux operating system. Approximately 30 sec elapse before the system is ready for operation and is ready to accept commands from the PC software. The boot status can be observed on the Zynq general-purpose input/output (GPIO) LEDs (L, C, R, and O). The correct sequence of events when the system boots up properly is as follows:
  - a. After SW1 is turned on, all four LEDs are on for approximately 15 sec. During this time, the image on the SD card is copied from the SD card to the FPGA memory.
  - b. Next, the LEDs begin flashing (moving the single on light), which indicates that the Linux operating system is booting up. The booting up process takes another 15 sec.
  - c. When the LEDs stop flashing, the system is ready for normal operation and awaits connection to the PC over Ethernet. Establish this connection using the TES.
  - d. The status of each LED during normal operation is as follows:
    - GPIO LED L: Receiver Link B synchronization.
    - GPIO LED C: Receiver Link A synchronization.
    - GPIO LED R: Transmitter Link B synchronization.
    - GPIO LED O: Transmitter Link A synchronization.
  - e. When shutdown is executed using the TES, the Linux operating system starts the power-down procedure. The power-down procedure requires a few seconds to complete. All four LEDs blinking together indicates that the user can safely power off the system using SW1 on the Zynq platform.
3. Connect the reference clock signal (30.72 MHz CW tone, 5 dBm maximum) to J401. After the TES is used to program the system, two LEDs on the [ADRV9008-1](#), [ADRV9008-2](#), and [ADRV9009](#) evaluation board (D401 and D402) are on. Active LEDs indicate that the correct reference clock is provided and phase-locked loops (PLLs) in the [AD9528](#) are locked.
4. For receiver testing on the [ADRV9008-1](#) and [ADRV9009](#) evaluation board, use a clean signal generator with low phase noise to provide an input signal to the selected RF input. Use a shielded RG-58, 50  $\Omega$  coaxial cable (1 m or shorter) to connect the signal generator.
  - a. To set the input level near the full scale of the receiver, set the generator level (for a single-tone signal) to approximately -15 dBm. This level depends on the input frequency and the gain settings through the path. There must be no input signal applied to the receiver input when performing an initialization calibration.
  - b. To set the input level near the full scale of the observation receiver, set the generator level (for a single-tone signal) to approximately -15 dBm. This level depends on the input frequency and the gain settings through the path.
5. For transmitter testing, connect a spectrum analyzer to either transmitter output on the [ADRV9008-2](#) or [ADRV9009](#) evaluation board. Use a shielded RG-58, 50  $\Omega$  coaxial cable (1 m or shorter) to connect the spectrum analyzer. Both transmitter paths must be terminated, either into spectrum analyzers, or if only one transmitter is being checked, the other transmitter must be terminated to 50  $\Omega$ . This termination is required because the initial calibrations run on both channels and can take a long time to complete if a transmitter channel is not correctly terminated.
6. Power off must be executed using the TES software or the user must power down the Zynq system using the SW9 push button (see Figure 1) before the user powers down the evaluation system by switching SW1 off.

It is important to note that the [ADRV9008-1](#), [ADRV9008-2](#), and [ADRV9009](#) evaluation system uses a Linux operating system. Linux requires time to boot up, as well as time to shut down before the hardware powers off. Use the software power-down feature or press the SW9 button on the Zynq platform before physically switching the power off using SW1. If this sequence is not used, the SD card may be corrupted and the [ADRV9008-1](#), [ADRV9008-2](#), and [ADRV9009](#) evaluation system may stop operating.

Perform correct shutdown by selecting **File > Shutdown Zynq platform** in the TES, or by pressing the SW9 push button on the Zynq platform.

After a few seconds, when all four GPIO LEDs on the Zynq platform blink together, the user can safely power off the system using SW1 on the Zynq platform.

## ADRV9008-1, ADRV9008-2, AND ADRV9009 TRANSCEIVER EVALUATION SOFTWARE (TES) INSTALLATIONS

Download the TES directly from the [design center landing page](#). After the initial software download, copy the software to the target system and unzip the files (if not already unzipped). The downloaded .zip file contains an executable file called **ADRV9009 Transceiver Evaluation Software.exe**.

Administrator privileges are required to install the TES. After running an executable file, a standard installation process follows. Parts of the installation build are Microsoft® .NET Framework 4.5 (which is mandatory for the software to operate) and IronPython 2.7.4 (which is optional and recommended). Figure 14 shows the recommended software installation configuration.

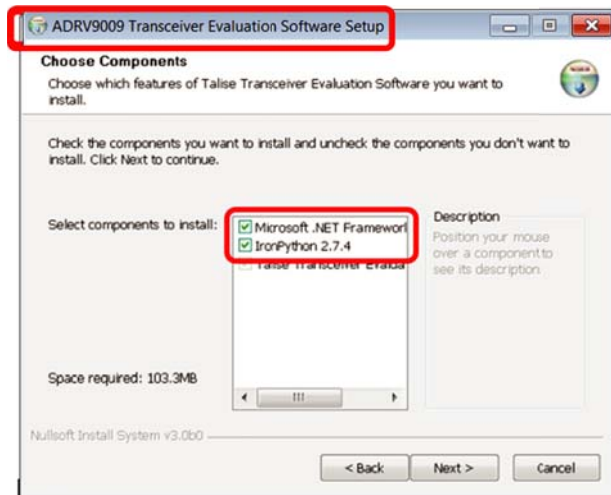


Figure 14. Software Installation Components

The last step of the installation process is to select the shortcut configuration (see Figure 15). The user can place the shortcut in the Windows start menu, or on the Windows desktop.

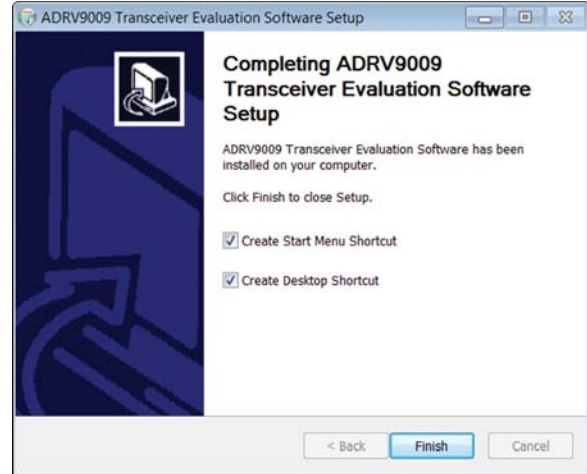


Figure 15. ADRV9009 Transceiver Evaluation Software Shortcut Configuration

## STARTING THE TRANSCEIVER EVALUATION SOFTWARE

Depending on the shortcut placement selection during the installation process (see Figure 15), the user can start the customer software by navigating to **Start > All Programs > Analog Devices > ADRV900x Transceiver Evaluation Software > ADRV9009 Transceiver Evaluation Software**, or by clicking on the **ADRV9009 Transceiver Evaluation Software** desktop shortcut. Figure 16 shows the opening page of the TES after it is activated.

### Demonstration Mode

Figure 16 shows the opening page of the TES. In a case when the evaluation hardware is not connected, the user can still use the software in demonstration mode by following this procedure:

1. Click **File > Connect** (top left corner of the TES).
2. The **Cannot Connect to Device** message appears. Click **OK** to proceed.
3. After clicking **OK**, the software enters demonstration mode, in which a superset of all transceiver family features is displayed.

The connection status is indicated at the bottom of the software window. When the status display reads **Disconnected**, the TES operates in demonstration mode (see Figure 17).

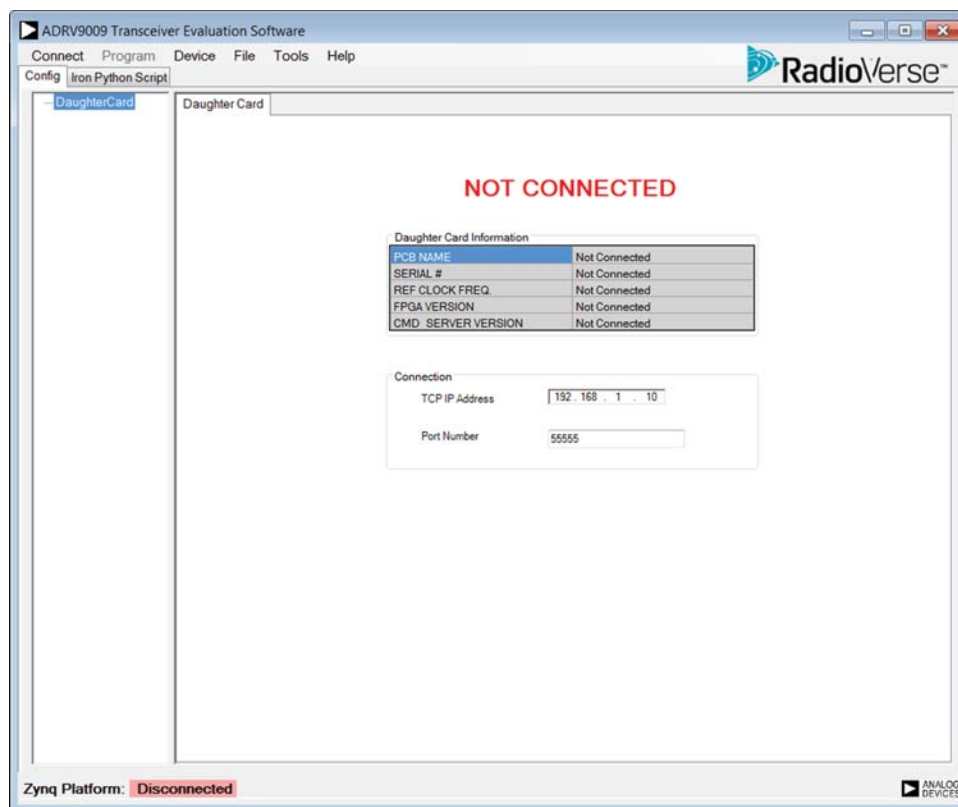


Figure 16. ADRV9009 TES Interface

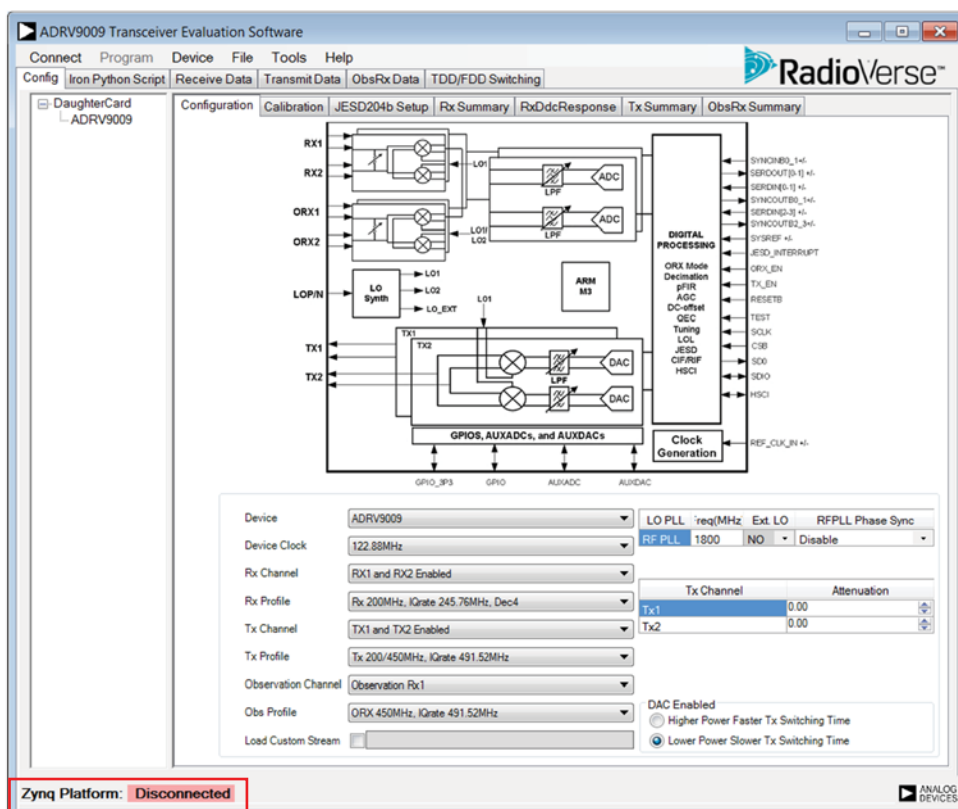


Figure 17. Project Setup Page of the ADRV9009 TES

## NORMAL OPERATION

To start using the complete evaluation system when the hardware is connected to a PC, click the **File > Connect** option in the drop-down menu at the top left of page to force the TES to establish a connection with the Zynq system via Ethernet. When a connection is established, click the **DaughterCard** position in the device tree on the left side of the window (see Figure 18). After selecting **DaughterCard**, information about the revisions of the different setup blocks appears in the main window. The bottom section of the window shows that the transfer control protocol (TCP) IP address set to 192.168.1.10 and that the port number is set to 55555. Contact Analog Devices if the [ADRV9008-1](#), [ADRV9008-2](#), and [ADRV9009](#) evaluation system must operate over a remote connection and a different IP address for the Zynq platform is desired.

Figure 18 shows an example of correct connection between a PC and a Zynq system with a daughter card connected to the Zynq system.

### Platform Files Update

Before continuing, determine if the latest version of the platform software is installed in the system. After the TES establishes a connection with the Zynq platform, the TES checks if the latest files are present. If the files must be updated, the TES informs the user.

Update the platform files by navigating to **Tools > Update > Platform Files**. The TES automatically updates files on the Zynq SD card and reboots the [ADRV9008-1](#), [ADRV9008-2](#), and [ADRV9009](#) evaluation system.

When all updates are installed, the system is ready for normal operation.

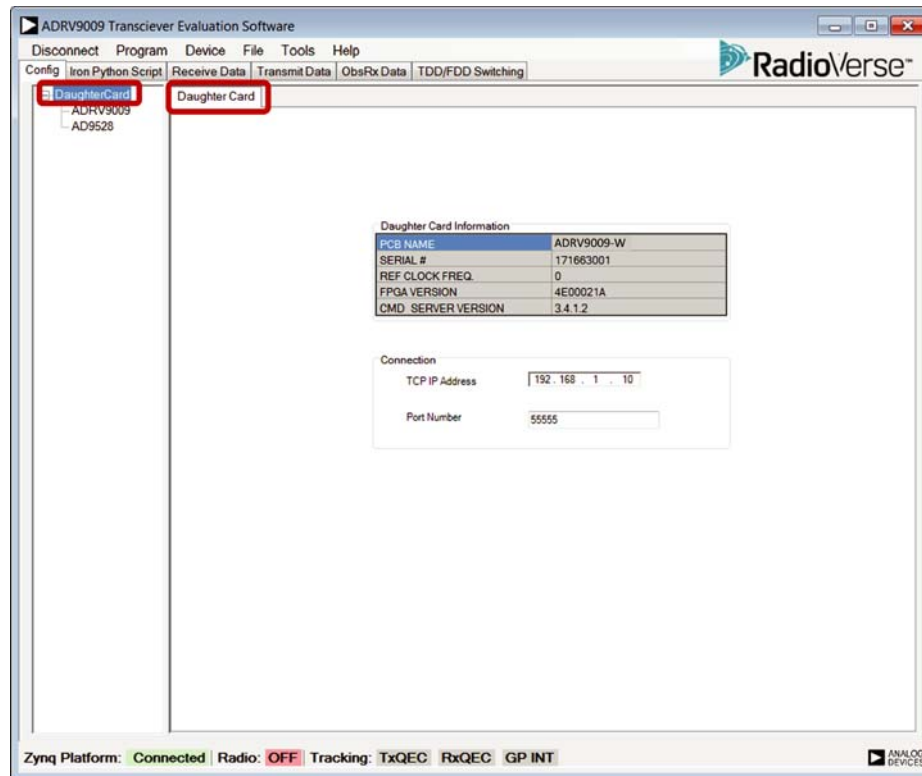


Figure 18. Setup Revision Information

### Configuring the ADRV9008-2 Transmitter

The TES contains five main user configurable pages (see Figure 19 to Figure 23). After the user selects **ADRV900x** in the device tree, the **Config** tab is activated. Contained within this tab are six sub tabs that contain setup options for the device. The first one displayed is the **Configuration** tab. Figure 19 shows the initial screen for the **ADRV9008-2**. In this page, the user can perform the following actions:

- Select the device to be programmed.
- Select the device clock frequency
- Select the number of active transmitter channels
- Select the profiles for the transmitter and observation receiver.
- Select the observation receiver channel
- Select the RF PLL frequency for the transmitter and observation receiver. An added feature allows the user to enable phase synchronization. This synchronization sets

the LO phase to a repeatable value for every change in the RF PLL frequency. Currently, only initialization and tracking continuously mode is supported. The RF PLL phase synchronization functionality is included at this time for prototyping and evaluation purposes only. Contact Analog Devices for function availability.

- Select the desired attenuation for the transmitter channels in dB.
- Load the custom stream. This feature assists customers in loading new stream files.
- Select the digital-to-analog converter (DAC) enabled. This section allows the user to either select a low power profile or a high power profile. The difference between the two profiles is that the DAC is left powered on while the transmitter is disabled (for a high power profile), and the DAC is disabled while the transmitter is disabled (for a low power profile). The only trade-off is the higher switching time required to turn on the DACs for the low power profile.

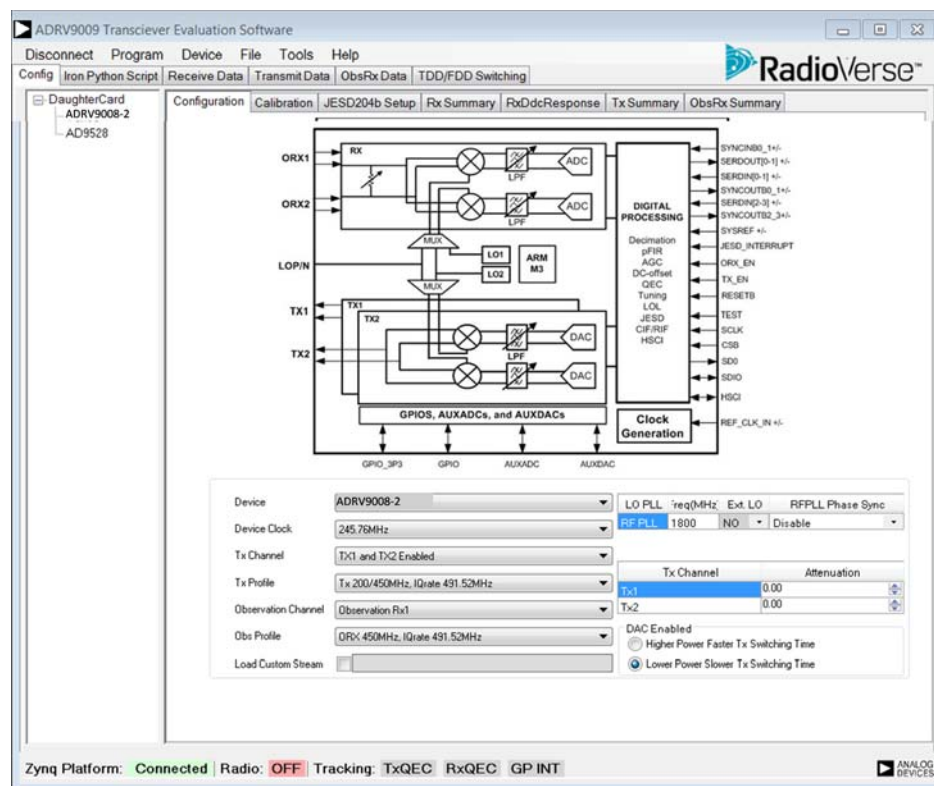


Figure 19. Main Configuration Tab for the ADRV9008-2

The second user configurable tab is the **Calibration** tab. The **Calibration** tab enables the initialization and tracking calibrations. Figure 20 shows a configuration example. The user can enable or disable initialization calibrations, as well as tracking calibrations. The initial calibrations, transmitter quadrature error correction (QEC) and internal transmitter LOL, along with the Transmitter 2 LOL, Transmitter 2 QEC, Observation Receiver 1 QEC, and Observation Receiver 2 QEC tracking calibrations can be enabled for the [ADRV9008-2](#) device. The user can also enable 3 dB DAC

boost mode in which the user can enhance the transmitter LOL performance. Using this mode, a further 3 dB margin is applied between the output signal and the LOL. The status bar at the bottom of the TES shows the status of the transmitter QEC tracking calibration and indicates whether the radio state is on or off. In addition, a section on the page allows the setup of receiver gain compensation mode, including the floating point options. Refer to the [ADRV9008-1-W/ADRV9008-2-W/ADRV9009-W Hardware Reference Manual](#) for more information.

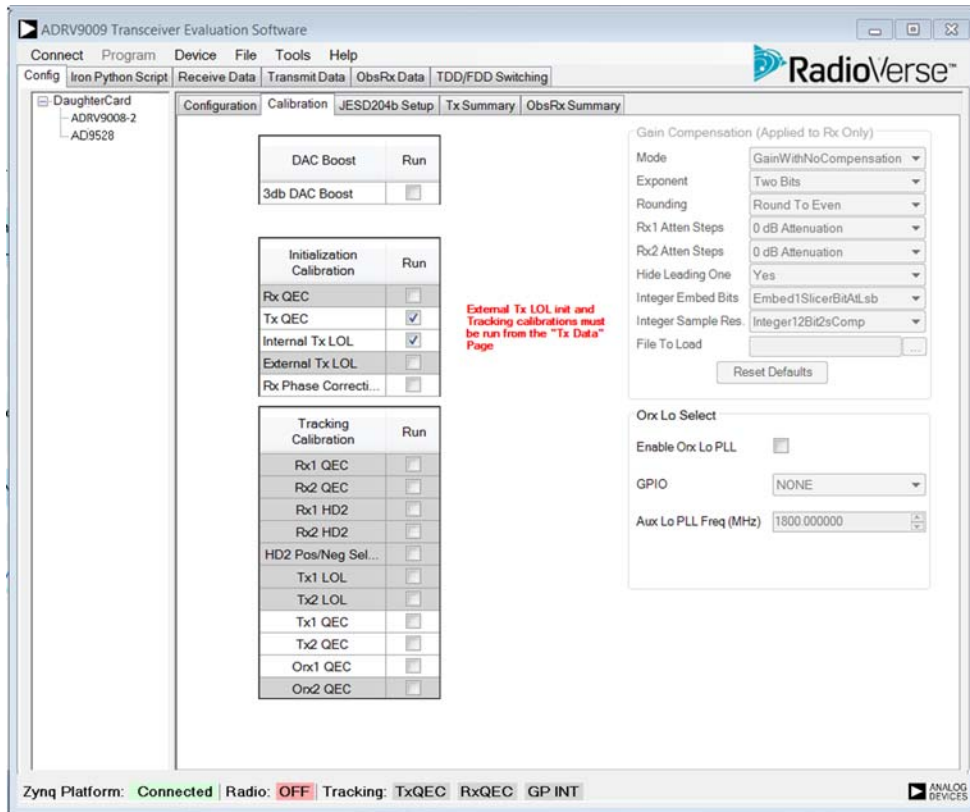


Figure 20. Calibration Configuration Tab for the [ADRV9008-2](#)



The third user configurable tab is the **JESD204b Setup** tab. The **JESD204b Setup** tab is used to set the characteristics of the digital data interface. Figure 21 shows a configuration example for the [ADRV9008-2](#). A subtab exists to select the receiver framer and the transmitter deframer. The user can set the desired JESD204B lane configuration, select scrambling, and choose whether to use an internal (free running) or external (provided by the [AD9528](#)) SYSREF signal to synchronize the

JESD204B links. The last check box in every framer/deframer is the option to relink on SYSREF. A feature is available to set the JESD204B lane rate as 11 Gbps. The Np parameter is set to 12 for 11 Gbps mode. This mode is currently only supported by the **Tx 200/300 MHz, IQrate 368.64MHz, Int5, 11G Tx profile** and the **ORX 300 MHz, IQrate 368.64MHz, Dec5, 12bit, 11G as ORx profile**.

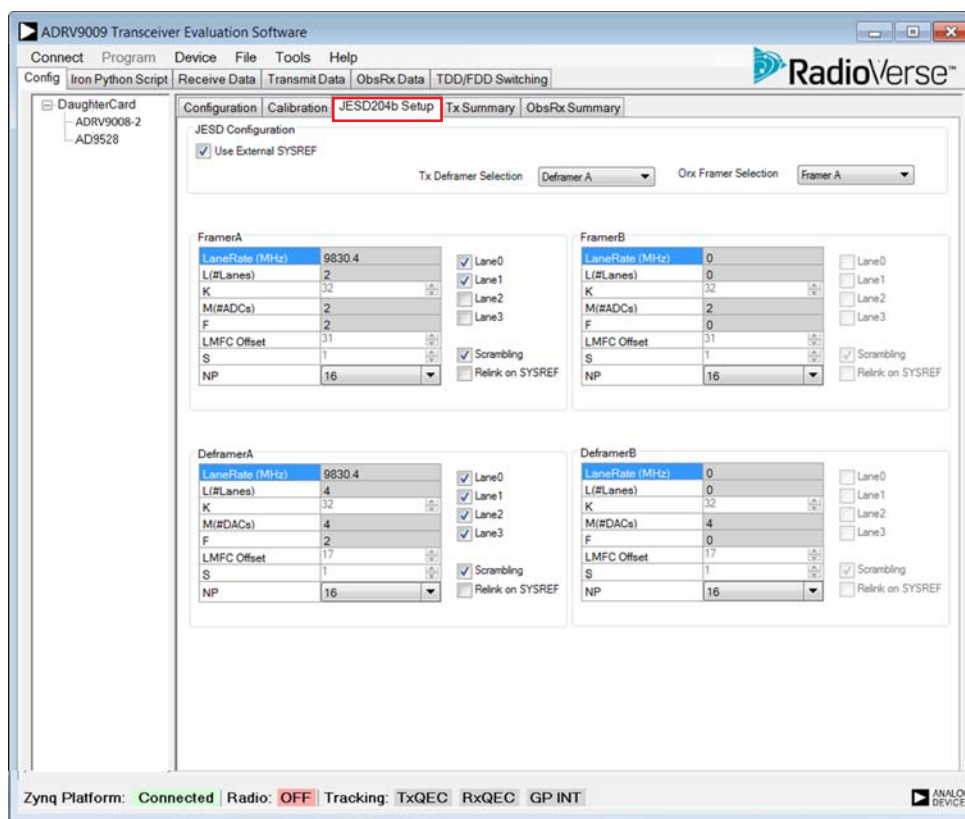


Figure 21. **JESD204b Setup** Tab for the [ADRV9008-2](#)

The **Tx Summary** tab and the **ObsRx Summary** tab are primarily informative and are based on the profile selection in the **Configuration** tab (see Figure 22 and Figure 23). In each tab, the user can check clock rates at each filter node, as well as filter characteristics and their pass-band flatness. Quick zooming capability allows zooming of the pass-band response, as well as the ability to restore the full-scale plot.

The TES also provides the capability to export the data plotted on the graphs to an external file. Perform this export action by right clicking the graph area and saving the data to a file for later analysis.

Figure 22 shows an example of the **Tx Summary** tab with the resulting composite filter response for the chosen profile.

Figure 23 shows an example of the **ObsRx Summary** tab.

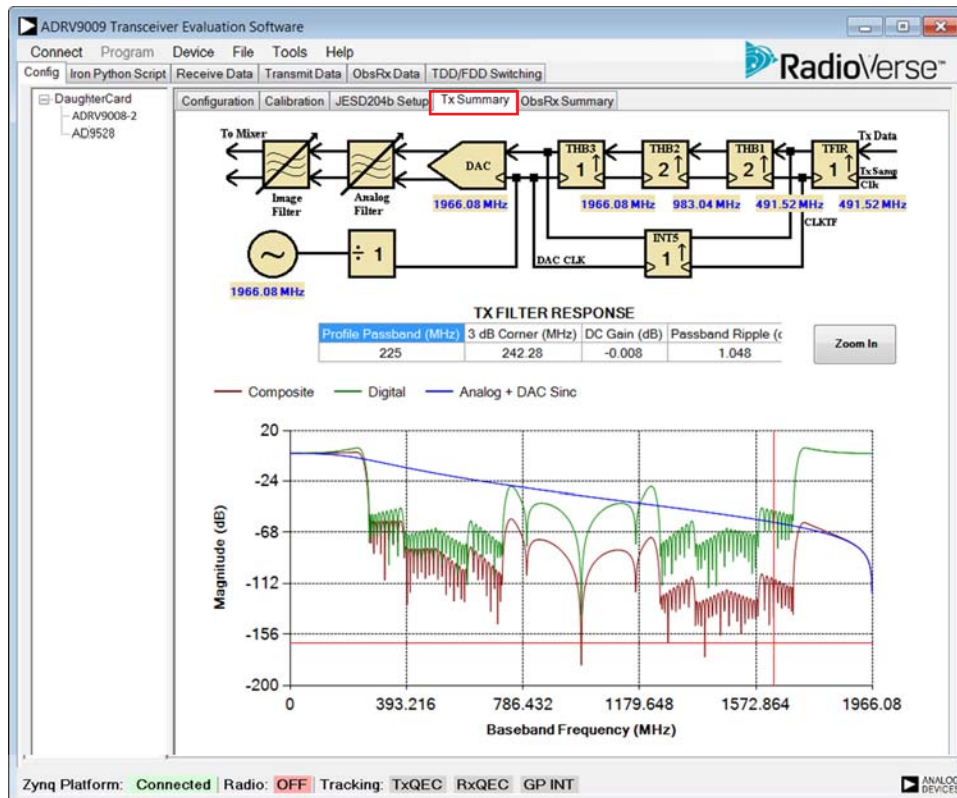


Figure 22. **Tx Summary** Tab

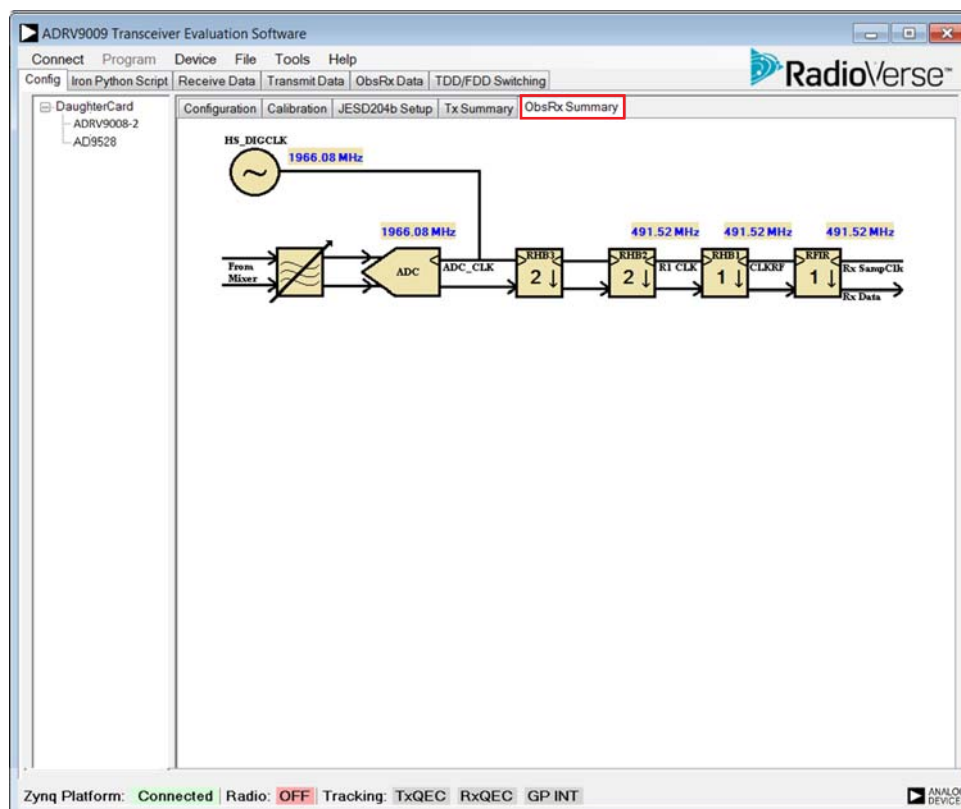


Figure 23. ObsRx Summary Tab

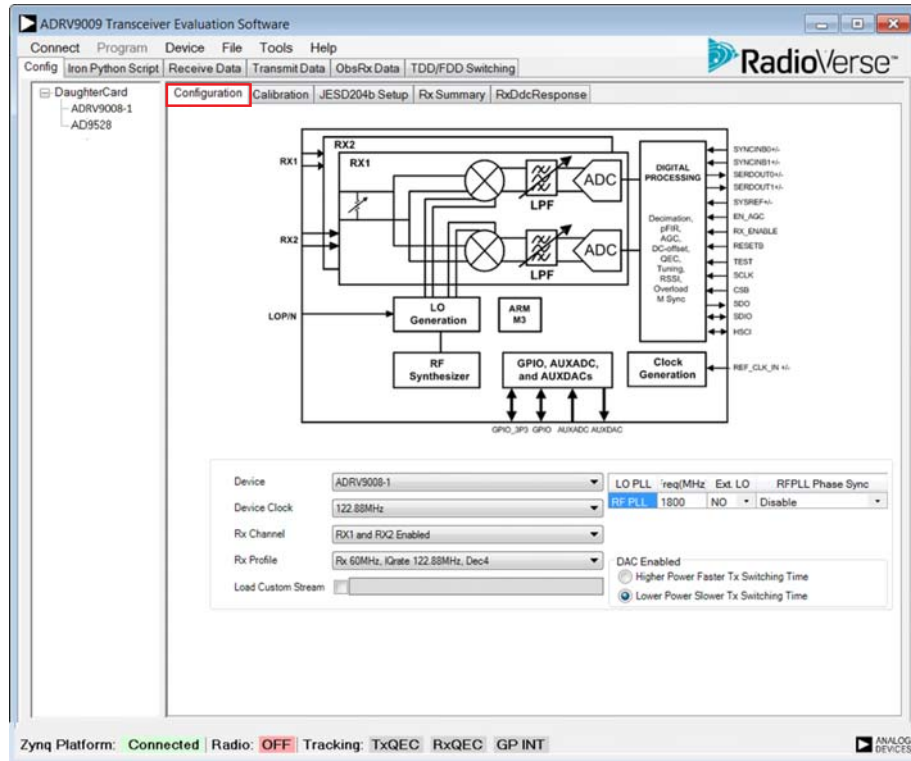


Figure 24. Main Configuration Tab for the ADRV9008-1

### Configuring the ADRV9008-1 Receiver

The TES contains four main user-configurable pages (see Figure 24 to Figure 27). After the user selects **ADRV9008-1** in the device tree, the **Config** tab is activated. Contained within this tab are six subtabs that contain setup options for the device. The first subtab displayed is the **Configuration** tab. Figure 24 shows the initial screen for the **ADRV9008-1** receiver. Depending on the device selected, the user can perform the following actions in this page:

- Select the device to be programmed.
- Select the device clock frequency.
- Select the number of active receiver channels.
- Select the profile for the receiver.
- Select RF PLL frequency for the receiver. A feature is available that allows the user to enable phase synchronization. This synchronization sets the LO phase to a repeatable value for every change in the RF PLL frequency. Currently, only initialization and tracking continuously mode is supported. The RF PLL phase synchronization functionality is included at this time for prototyping and evaluation purposes only. Consult Analog Devices for function availability.
- Load the custom stream. This feature is added to assist customers in loading new stream files.
- Select the desired DAC enabled option. This section allows the user to either select a low power profile or a high power profile. The difference between the two profiles is that the DAC is left powered on during transmitter disable (for a high power profile) and is disabled during transmitter disable (for a low power profile). The only trade-off is the higher switching time required to turn on the DACs for the low power profile. This selection does not have any effect for the **ADRV9008-1**.

The second user configurable tab is the **Calibration** tab. The **Calibration** tab is used to enable initialization and tracking calibrations. Figure 25 shows a configuration example. The user can enable or disable initialization calibrations, as well as tracking calibrations. The initial calibrations, receiver QEC, along with the Receiver 1 QEC and Receiver 2 QEC tracking calibrations can be enabled for the [ADRV9008-1](#) receiver device (see Figure 25). A calibration receiver HD2 canceller feature is available. Due to conflicting resources required by the receiver QEC and receiver HD2, currently only one of the two calibrations can be activated at an instant. The status bar at the bottom of the TES shows the

status of the QEC receiver tracking calibration and indicates if the radio state is on or off. A new section is available to enable floating point mode. In addition, a section on the page allows the setup of receiver gain compensation mode, including the floating point options. Refer to the [ADRV9008-1-W/ADRV9008-2-W/ADRV9009-W Hardware Reference Manual](#) for more information.

The user can also enable the 3 dB DAC boost mode, in which the user can enhance the transmitter LOL performance. Using this mode, a further 3 dB margin is applied between the output signal and the LOL.

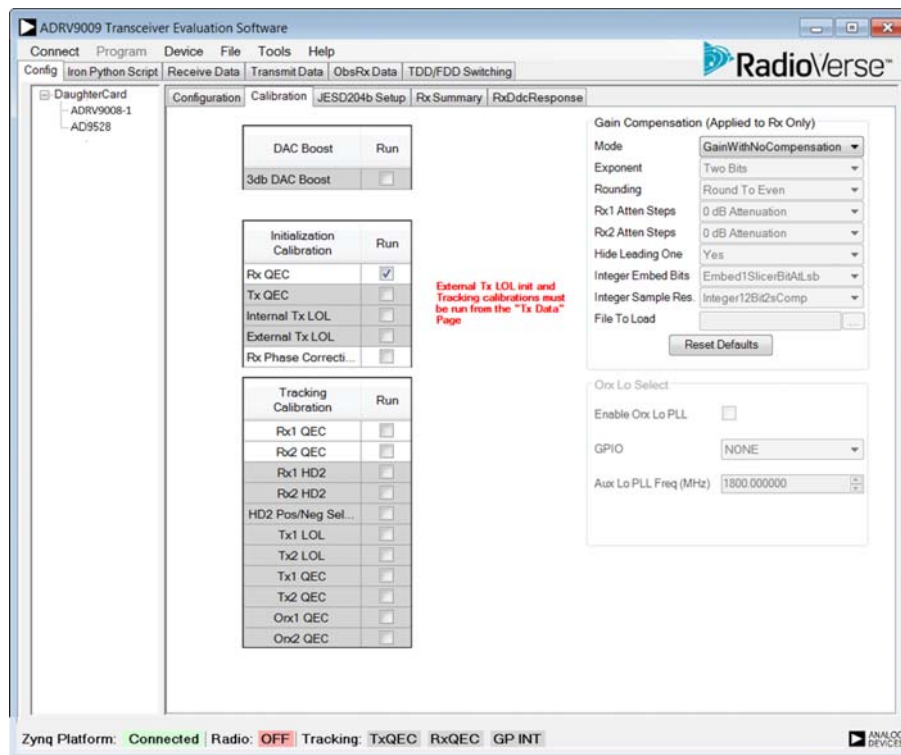


Figure 25. Calibration Configuration Tab for the [ADRV9008-1](#)

The third user configurable tab is **JESD204b Setup** and is used to set the characteristics of the digital data interface. Figure 26 shows a configuration example for the [ADRV9008-1](#), [ADRV9008-2](#), and [ADRV9009](#) receiver. A subtab exists to select the receiver framer and the transmitter deframer. The user can set the desired JESD204B lane configuration, select scrambling, and whether to use an internal (free running) or external (provided by the

[AD9528](#)) SYSREF to synchronize the JESD204B links. The last check box in each framer/deframer is the option to relink on SYSREF. A feature is available to set the JESD204B lane rate as 11 Gbps. The Np parameter is set to 12 for 11 Gbps mode. This mode is currently only supported by the **Rx 205 MHz, IQrate 368.64MHz, Dec5 receiver profile**.

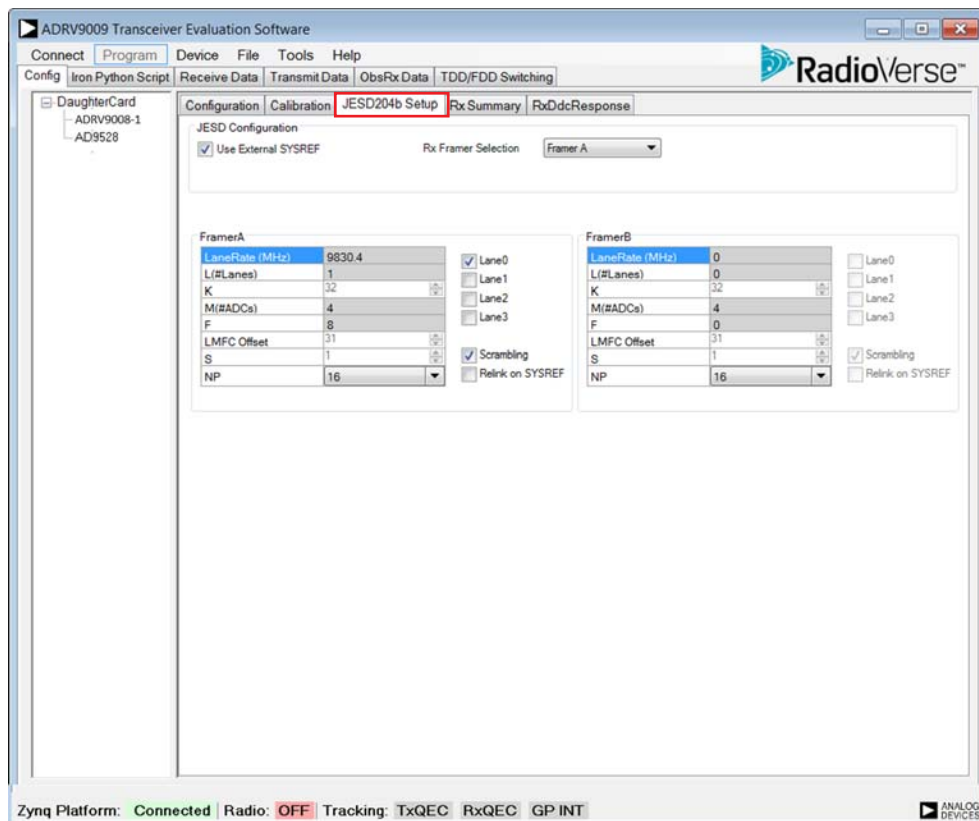


Figure 26. JESD204b Setup Tab for the [ADRV9008-1](#)



The **Rx Summary** tab is primarily informative and is based on the profile selection in the **Configuration** tab (see Figure 27). In each of these tabs, the user can check clock rates at each filter node, as well as filter characteristics and their pass-band flatness. Quick zooming capability allows zooming of the pass-band response, as well as the ability to restore the full-scale plot. The TES also provides the capability to export the data plotted on the graphs to an external file. Perform this export by right clicking on the graph area and saving the data to a file for later analysis. Figure 27 shows an example of the **Rx Summary** tab with the resulting composite filter response for the chosen profile.

The receiver uses square wave mixing to downconvert the receive signal to baseband. Square wave mixing also downconverts signals around the odd harmonics of the receiver LO signal. Spurious signals around odd harmonics of the LO must be filtered to prevent interference with the receive signal. Spurious signals that generate harmonics that fall around odd harmonics of the LO must also be filtered to prevent spurious harmonics from interfering with the receive signal.

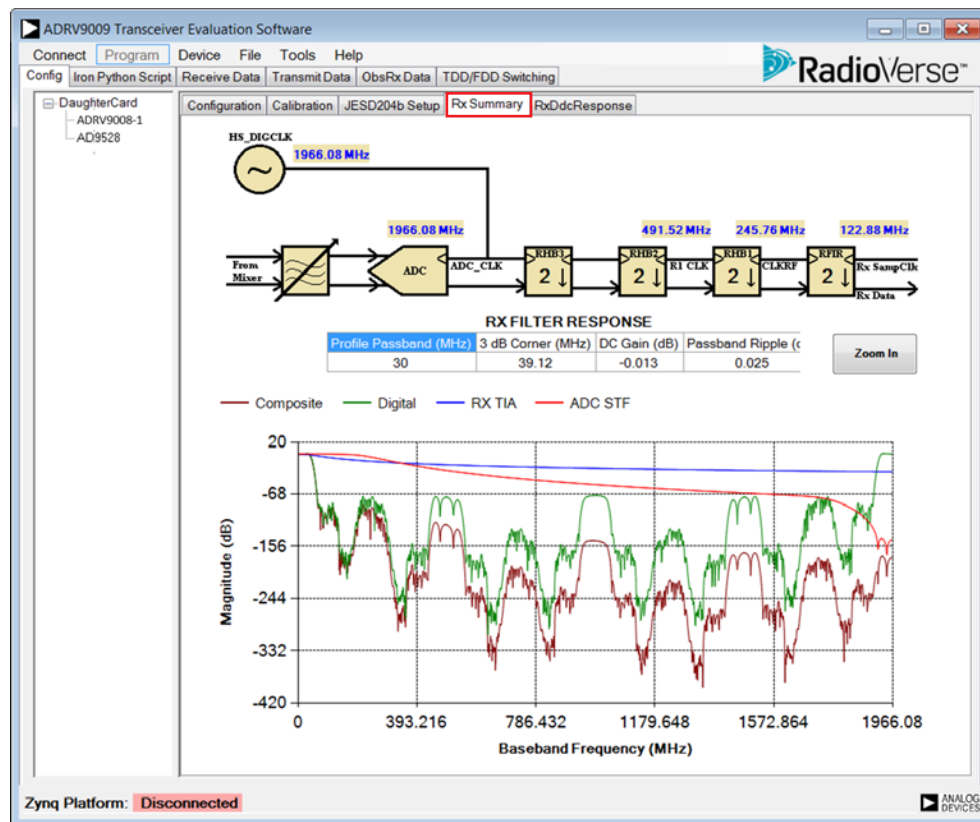


Figure 27. Rx Summary Tab

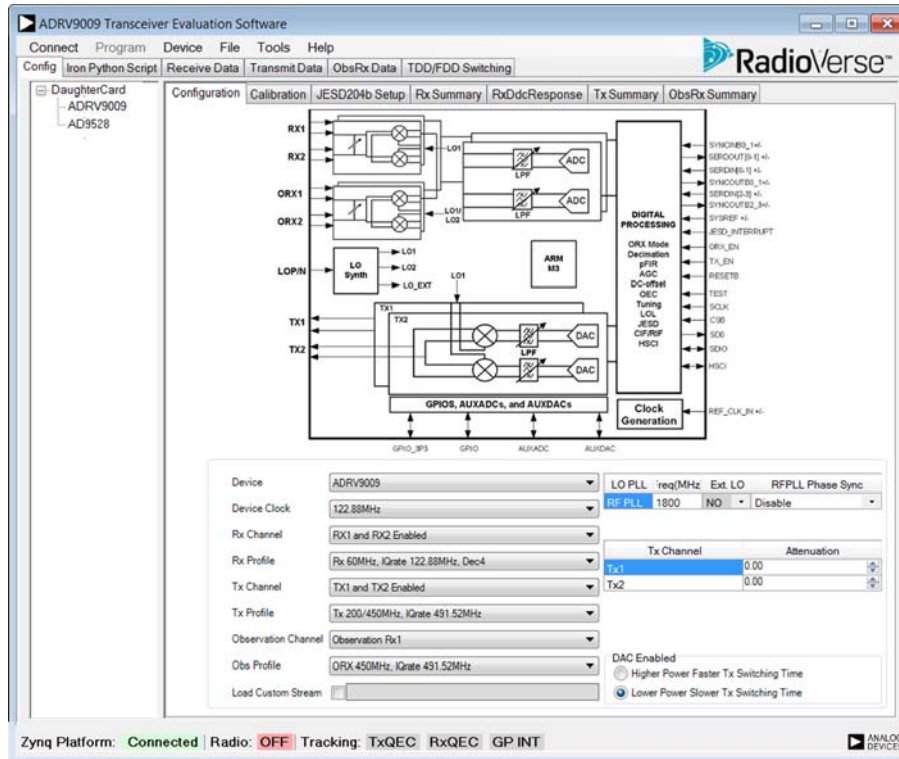


Figure 28. Main Configuration Tab for the ADRV9009 TDD

### Configuring the ADRV9009 TDD Device

The TES contains five main user-configurable pages (see Figure 22, Figure 23, and Figure 27 to Figure 30). After the user selects the ADRV9009 in the device tree, the **Config** tab is activated.

Contained within this tab are subtabs that contain setup options for the device. The first subtab displayed is the **Configuration** tab. Figure 28 shows the initial screen for the ADRV9009 TDD device. The user can perform the following actions in this page:

- Select the device to be programmed.
- Select the device clock frequency.
- Select the number of active transmitter channels.
- Select the profiles for the transmitter and observation receiver.
- Select the observation receiver channel.
- Select the number of active receiver channels.
- Select the profile for the receiver.
- Select RF PLL frequency for the receiver. A feature is available that allows the user to enable phase synchronization. This synchronization sets the LO phase to a repeatable value for every change in the RF PLL frequency. Currently, only initialization and tracking continuously mode is supported. The RF PLL phase synchronization functionality is included at this time for prototyping and evaluation purposes only. Consult Analog Devices for function availability.
- Select the desired attenuation for the transmitter channels in dB.
- Load the custom stream. This feature assists customers in loading new stream files.
- Select the DAC enabled. This section provides the user the capability to either select a low power profile or a high power profile. The difference between the two profiles is that the DAC is left powered on during transmitter disable (for the high power profile) and is disables during transmitter disable (for the lower power profile). The only trade-off is the higher switching time required to turn on the DACs for the lower power profile.

The second user configurable tab is the **Calibration** tab. The **Calibration** tab is used to enable the initialization and tracking calibrations. Figure 29 shows a configuration example. The user can enable or disable initialization calibrations, as well as tracking calibrations. The initial calibrations, transmitter QEC, receiver QEC, and internal transmitter LOL, along with the Receiver 1 QEC, Receiver 2 QEC, Transmitter 2 LOL, Transmitter 2 LOL, Transmitter 2 QEC, Observation Receiver 1 QEC and Observation Receiver 2 QEC tracking calibrations can be enabled for the [ADRV9009](#) (see Figure 29). The user can also enable 3 dB DAC boost mode, in which the user can enhance the transmitter LOL

performance. Using this mode, a further 3 dB margin is applied between the output signal and the LOL. The status bar at the bottom of the TES shows the status of the transmitter QEC and receiver QEC tracking calibration and indicates whether the radio state is on or off. A section is available to enable floating point mode. In addition, a section on the page allows the setup of receiver gain compensation mode, including the floating point options. Refer to the [ADRV9008-1-W/ADRV9008-2-W/ADRV9009-W Hardware Reference Manual](#) for more information.

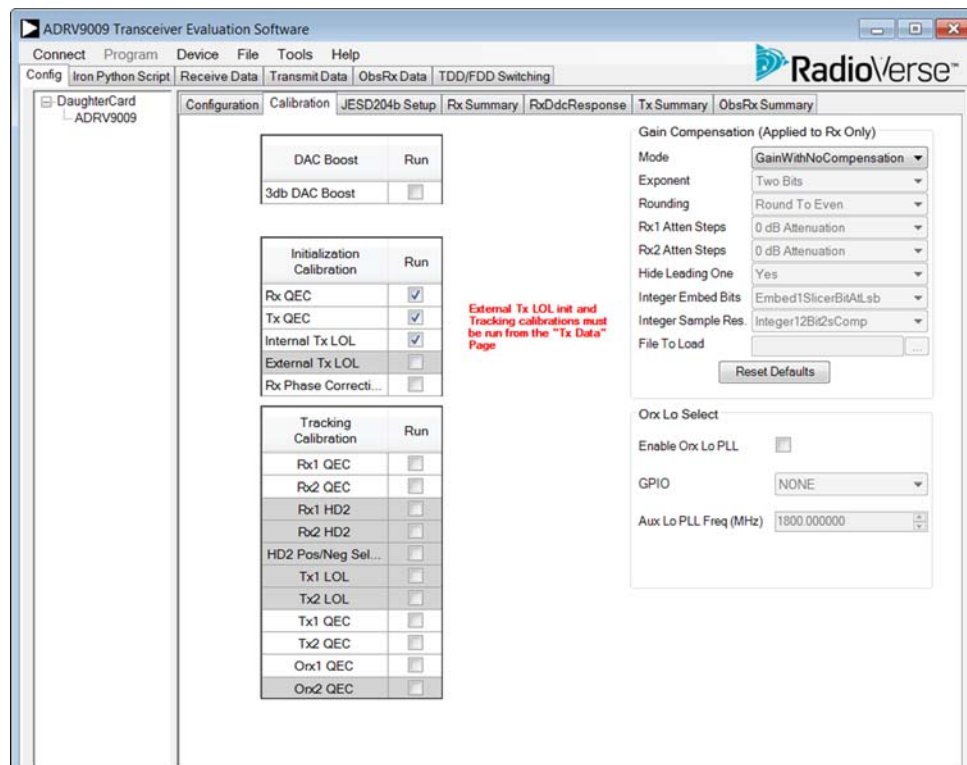


Figure 29. Calibration Configuration Tab for the [ADRV9009](#)

The third user configurable tab is the **JESD204b Setup** tab. The **JESD204b Setup** tab is used to set the characteristics of the digital data interface. Figure 30 shows a configuration example for the [ADRV9009](#). A subtab exists to select the receiver framer and the transmitter deframer. The user can set the desired JESD204B lane configuration, select scrambling, and whether to use an internal (free running) or external (provided by the [AD9528](#)) SYSREF to synchronize the JESD204B links. The last check box in each framer/deframer is the option to relink on SYSREF. A feature is available to set the JESD204B lane rate as 11 Gbps. The Np parameter is set to 12 for 11 Gbps mode. This mode is currently only supported by the **Tx 200/300 MHz, IQrate 368.64MHz, Int5, 11G Tx profile, the Rx 205 MHz,**

**IQrate 368.64MHz, Dec5 as Rx profile, and the ORX 300 MHz, IQrate 368.64MHz, Dec5, 12bit, 11G as ORx profile.**

Configure the JESD204B section for [ADRV9009](#) as follows:

- The receiver framer selection must be set to Framer A.
- The observation receiver framer selection must be set to Framer B.
- The transmitter deframer selection can be set to either Deframer A or Deframer B.
- Ensure that the lane rates for Framer A and Observation Receiver Framer B are the same.
- Ensure that Framer A and Observation Receiver Framer B do not use the same lanes.

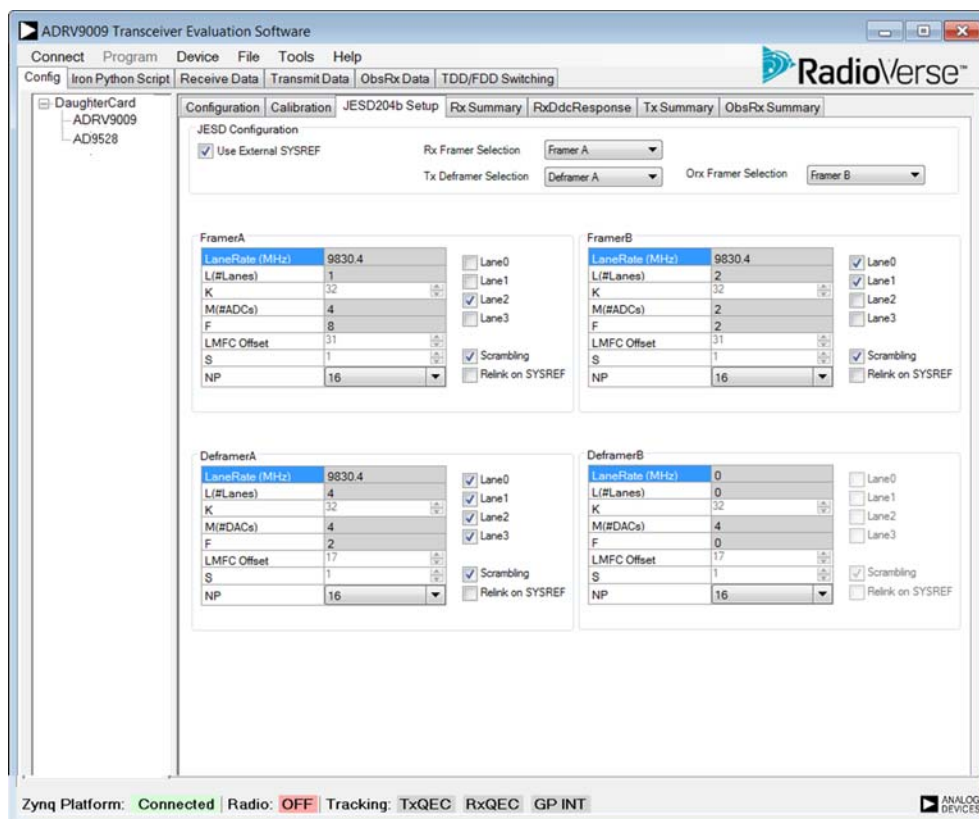


Figure 30. **JESD204b Setup** Tab for the [ADRV9009](#)

The **Tx Summary** tab, **Rx Summary** tab, and **ObsRx Summary** tab are primarily informative and are based on the profile selection in the **Configuration** tab (see Figure 28). In each tab, the user can check clock rates at each filter node, as well as filter characteristics and their pass-band flatness. Quick zooming capability allows zooming of the pass-band response, as well as the ability to restore the full-scale plot. The TES also provides the capability to export the data plotted on the graphs to an external file. Perform this export by right clicking on the graph area and saving the data to a file for later analysis. Figure 22 shows an example of the **Tx Summary** tab with the resulting composite filter response for the chosen profile.

Figure 23 shows an example of the **ObsRx Summary** tab. Figure 27 shows an example of the **Rx Summary** tab with the resulting composite filter response for the chosen profile.

### Configuring the AD9528

The daughter card uses the **AD9528** clock chip to provide the reference clock (REF\_CLK), as well as a SYSREF pulse to the **ADRV9008-1**, **ADRV9008-2**, and **ADRV9009** and the FPGA via the FMC connector. The **AD9528** can be configured using the **Clock Setup** tab, as shown in Figure 31. The input reference frequency can be selected from a drop-down menu. The user must provide an external reference clock to the J401 SMA connector that matches the frequency selected in the drop-down menu. The signal amplitude must not exceed 5 dBm.

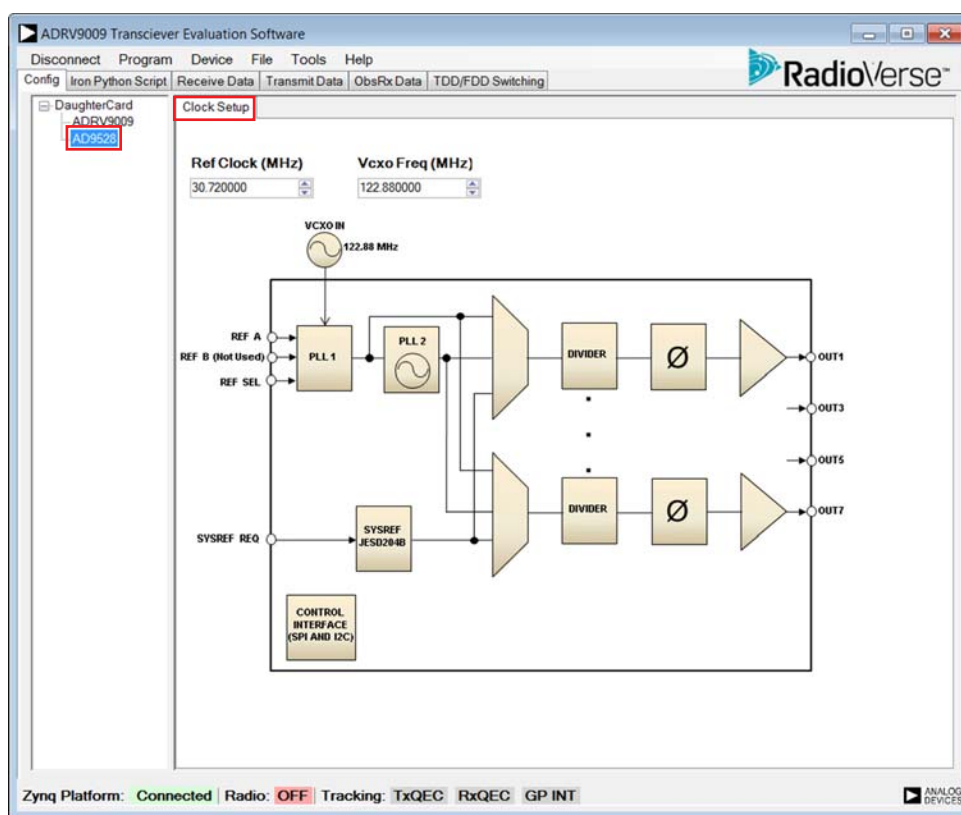


Figure 31. AD9528 Configuration Page

### Programming the Evaluation System

After all tabs are configured, the user must press the **Program** button. After pressing the **Program** button, TES sends a series of API commands that are executed by a dedicated Linux application on the Zynq platform.

When programming completes, the system is ready to operate. A progress bar appears at the bottom of the window. Figure 32 displays the window with the progress bar and the message that appears after the device is successfully programmed. If an error or warning message appears instead, see the Error Handling section to search for troubleshooting guidelines.

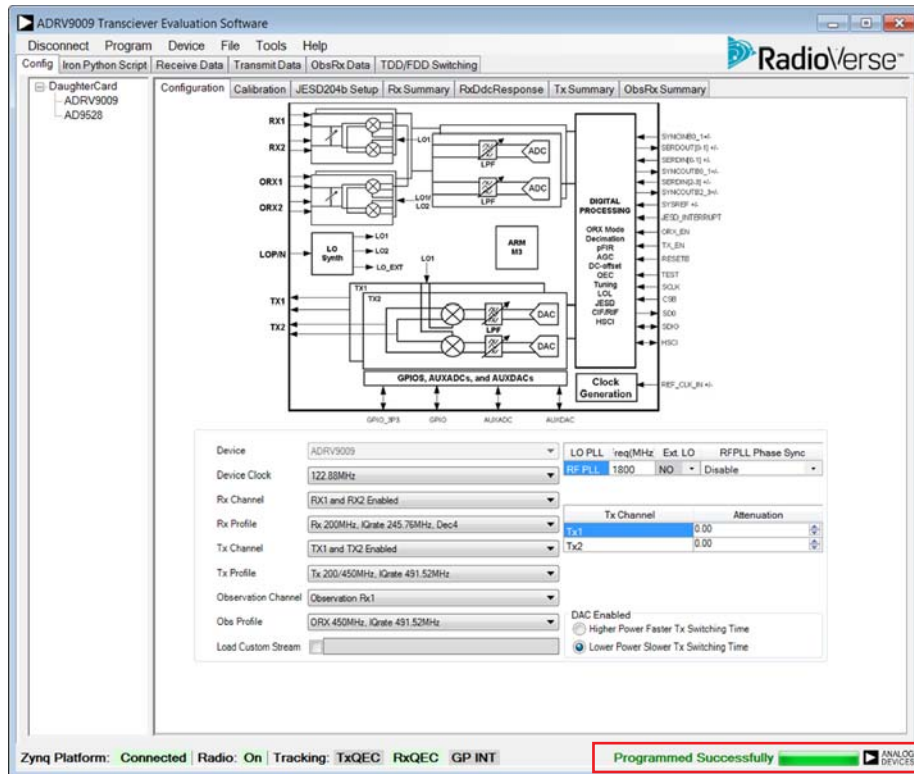


Figure 32. Programming the Device Successfully



## OTHER TES FEATURES

### Save/Load Profile

The TES allows the user to store and load all configuration settings described in the Normal Operation section. To save software settings, click the **File > Save GUI Setup** option, shown in Figure 33. The TES generates a **.xml** format file with all software settings recorded. The user can then load software settings by clicking the **File > Load GUI Setup** option and selecting the saved setup file. The load custom profile function can be used to load profiles generated by the [ADRV9008-1](#), [ADRV9008-2](#), and [ADRV9009](#) filter wizard.

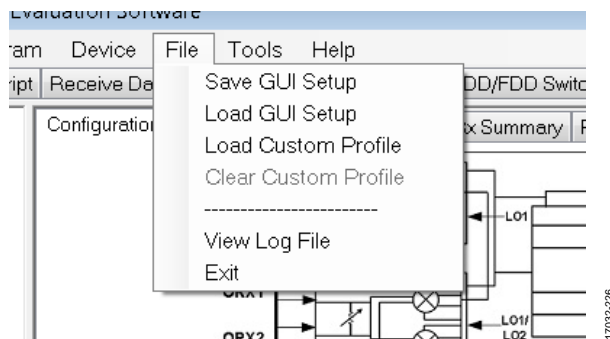


Figure 33. Configuration Menu Control Buttons

### ADRV9008-1, ADRV9008-2, and ADRV9009 Initialization Script

The TES allows the user to create a script with all API initialization calls in the form of IronPython functions. When the user clicks the **Tools > Save Python Script** option, the script can be given a file name and stored in a location (chosen by the user) for

future use. The TES generates the script in the form of an IronPython (**.py**) file. This file can then be executed using the **IronPython Script** tab shown in Figure 43. There is an option to save a MATLAB-based initialization script for the chosen setup in the GUI.

### API Configuration Structure Initialization

Based on the configuration settings described in the previous sections, the TES sets up structure member values that are then used by API commands. The TES allows the user to create a **\*.c** file that contains all of these initial values. This file can be imported into a user system that uses the [ADRV9008-1](#), [ADRV9008-2](#), and [ADRV9009](#) APIs. To generate the **\*.c** files, the user must click the **Tools > Save .c Init Script** option. This action opens the **Save As** window, requiring the user to name the file and specify a location for storage. The TES generates files as follows:

- **headless.c**. This file provides an example file that makes calls into the [ADRV9008-1](#), [ADRV9008-2](#), and [ADRV9009](#) API to initialize the [ADRV9008-1](#), [ADRV9008-2](#), and [ADRV9009](#) device.
- **headless.h**. This file is a header file for **headless.c**.
- **user\_name.c**. This file contains all initialization values for the structure members used by the [ADRV9008-1](#), [ADRV9008-2](#), and [ADRV9009](#) APIs.
- **user\_name.h**. This file is a header file for **user\_name.c**.
- **user\_name\_ad9528init.c**. This file contains all initialization values for the structures used by the [AD9528](#) (clock IC) APIs.

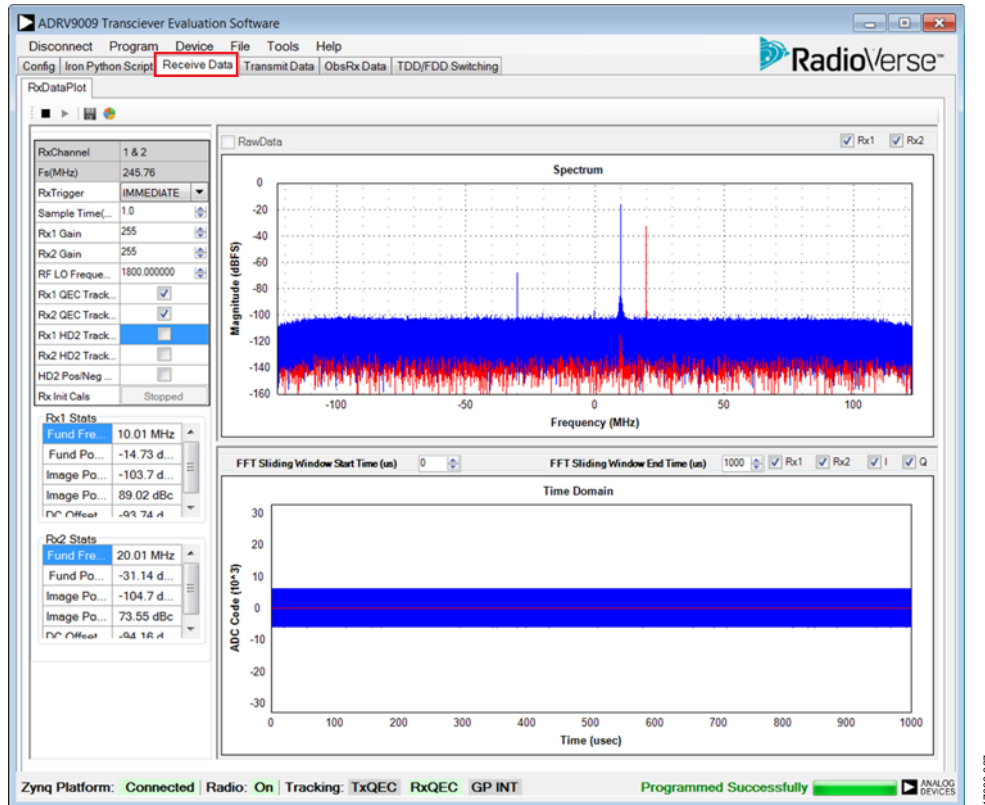


Figure 34. Receive Data Tab

## RECEIVER SETUP

### Receiver Signal Chain

After configuring software using the **Config** tab and selecting **Program**, the system is ready for normal operation. Selecting the **Receive Data** tab opens a page as shown in Figure 34. After the **Receive Data** tab is open, the user can enter the RF receiver center frequency in MHz. The receiver gain can be set by entering the desired gain index for each receiver channel. The gain index refers to the value in the programmable gain index table. Refer to the [ADRV9008-1-W/ADRV9008-2-W/ADRV9009-W Hardware Reference Manual](#) for gain index table specifics.

By pressing the play symbol in the **Receiver Data** tab, the transceiver moves to the receive state and graphs received data in both frequency and time domains. An example of a captured waveform is shown in Figure 34. The upper plot displays the FFT result and the lower plot shows the time domain waveform. If the FFT analysis is selected (by clicking the multicolored pie chart symbol), basic analysis information from the FFT is displayed on the left side of the screen. The status bar at the bottom of the TES shows the status of the receiver QEC and indicates whether the radio state is on or off.

The receiver trigger drop-down menu can be used to select an immediate trigger, an external trigger, or a TDD state machine pulse. The drop-down menu options are as follows:

- The **IMMEDIATE** option starts the capture as soon as the SPI command is received to initiate a capture operation.
- The **EXT\_SMA** option starts the capture when a high level is present at Connector J68 on the Zynq platform.
- The **TDD\_SM\_PULSE** option starts the capture, depending on the current state of the TDD state machine.

The received data can be saved to a file by clicking the floppy disk icon. Selecting this option displays a window allowing the user to select the format for the exported data. If the file type is specified to be Agilent© data, the TES adds a header to the saved file that allows Agilent vector signal analyzer (VSA) software to use the header to read and demodulate the data. The header is followed by data stored in I/Q format. Other formats supported by software are I Q (no header information) or I, Q (no header information). The number of points saved to the file is determined by the number of samples selected in the **# Samples** box.

The TES allows the user to obtain the FFT of a particular time slot by using the **FFT Sliding Window Start Time (us)** box and the **FFT Sliding Window End Time (us)** box. These functions allow the FFT to be calculated only for the selected time slot. The **FFT Sliding Window Start Time (us)** box denotes the start time of the FFT sliding window, whereas the **FFT Sliding Window End Time (us)** box denotes the end time of the FFT sliding window. The FFT sliding window start time must be greater than zero and less than the FFT sliding window end time. The FFT sliding window end time must be less than the maximum time shown in the time domain graph of the TES.

The user can also rerun initial receiver calibrations by pressing the **Rx Init Cals** button. When calibrations are finished, the button changes appearance to display a stopped condition. Note that there must be no input signal applied to the receiver input when performing an initialization calibration. Use initialization calibrations when the image rejection must be high.

The user can also enable or disable QEC tracking calibrations. The **Rx1 QEC Tracking** tick box enables calibration for the Receiver 1 path and the **Rx2 QEC Tracking** tick box enables calibration for the Receiver 2 path. Tracking calibrations operate when a receiver signal path receives real data.

### Observation Receiver Signal Chain

Selecting the **ObsRx Data** tab opens a page as shown in Figure 35. The observation receiver gain can be set by entering the desired gain index. The gain index refers to the value in the programmable gain index table. Refer to the [ADRV9008-1-W/ADRV9008-2-W/ADRV9009-W Hardware Reference Manual](#) for gain index table specifics.

After pressing the play symbol in the **ObsRx Data** tab, the [ADRV9008-2](#) or [ADRV9009](#) moves to the receive state and graphs the output data. An example of a captured waveform is shown in Figure 35.

The received data can be saved to a file by clicking the floppy disk icon. Selecting this option displays a window allowing the selection of the format for the exported data. If the file type is specified to be Agilent data, the TES adds a header to the saved file that can be read by the Agilent VSA software and used to demodulate the data. The header is followed by data stored in I <TAB> Q [new\_line] format. Other formats supported by software are I <TAB> Q [new\_line] (no header information) or I,Q [new\_line] (no header information). The number of points saved to the file is determined by the number of samples selected in the **# Samples** box.

The TES allows the user to obtain the FFT of a particular time slot by using the **FFT Sliding Window Start Time (us)** box and the **FFT Sliding Window End Time (us)** box. These functions allow the FFT to be calculated only for the selected time slot. The **FFT Sliding Window Start Time (us)** box denotes the start time of the FFT sliding window, whereas the **FFT Sliding Window End Time (us)** box denotes the end time of the FFT sliding window. The FFT sliding window start time must be greater than zero and less than the FFT sliding window end time. The FFT sliding window end time must be less than the maximum time shown in the time domain graph of the TES.

To start operation of the observation receiver signal path, the **Radio On** button must be enabled.

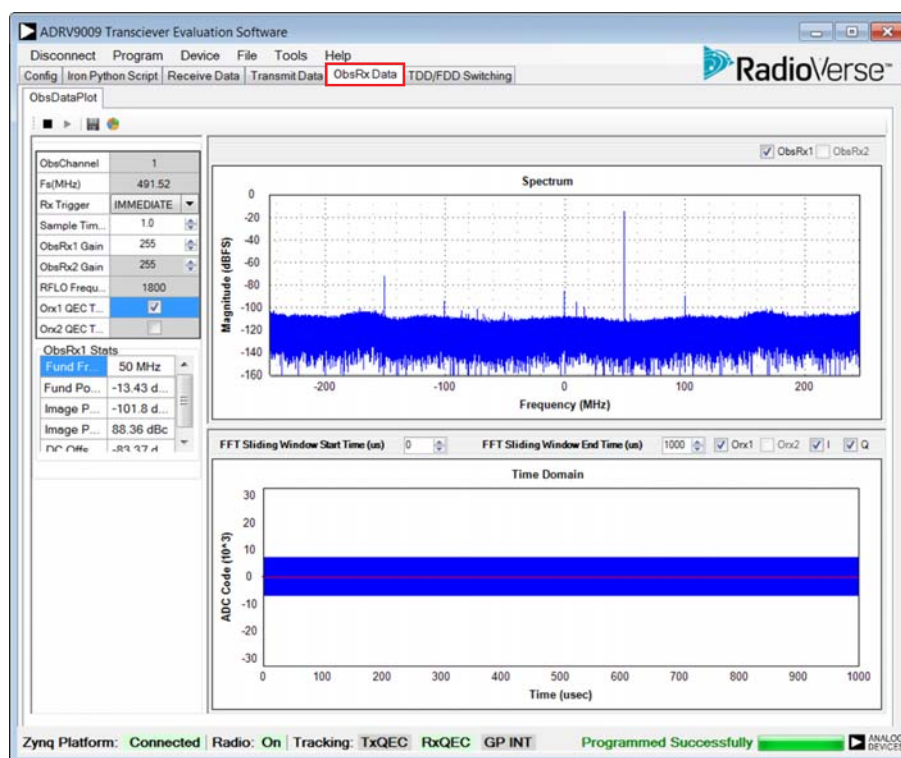


Figure 35. **ObsRx Data** Tab

## TRANSMITTER SETUP

Selecting the **Transmit Data** tab opens a page as shown in Figure 36. The upper plot displays the FFT of the digital input data, and the lower plot shows the time domain waveform. When the Transmitter 2 outputs are enabled, the user can select the Transmitter 2 data to be displayed in the spectrum plot. In the time domain plot, the user can select Transmitter 2, I, or Q data to be displayed.

After the **Transmit Data** tab is open, the user can enter the RF transmitter center frequency in MHz, change the attenuation level, enable different calibrations, control data scaling, and transmit CW tones. The status bar at the bottom of the TES shows the status of the transmitter QEC and indicates whether the radio state is on or off.

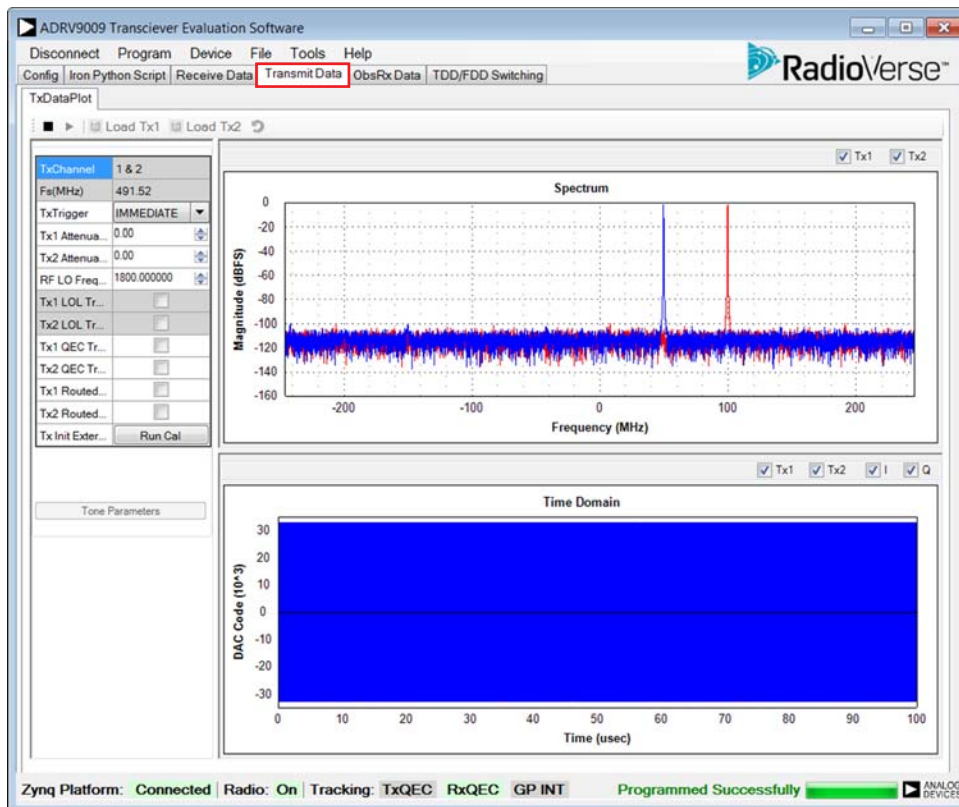


Figure 36. **Transmit Data** Tab

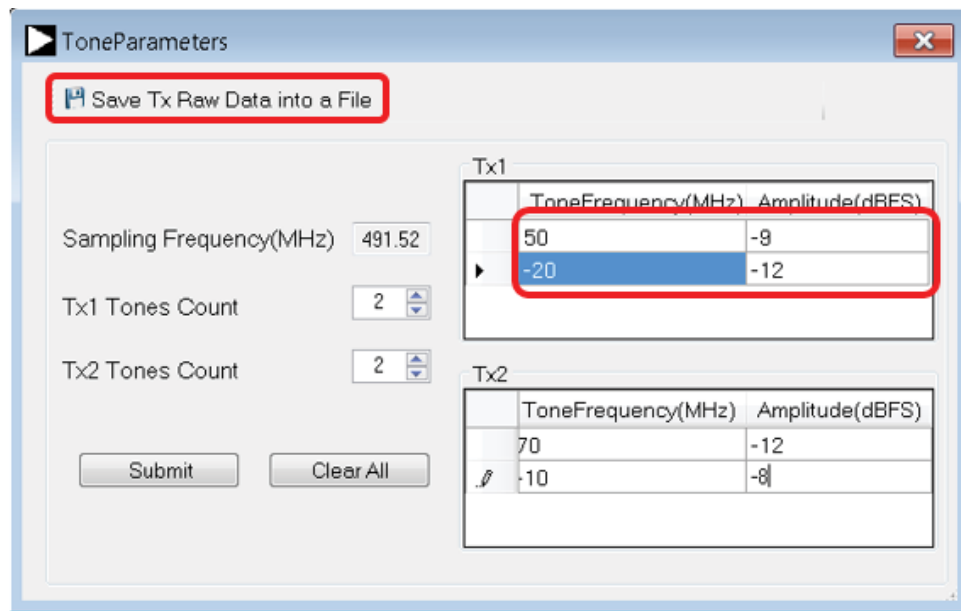


Figure 37. Transmitter Tone Parameters Setup Menu

### Transmitter Data Options

The TES provides the following options for inputting transmitter data:

- A single tone or two tones can be generated by the evaluation system using the **ToneParameters** menu shown in Figure 37. In this window, the user can select the number of tones (1 or 2) to be transmitted on the selected transmitter output. The user has control over the tone frequency offset with respect to the LO frequency and tone amplitude in dBFS. The user can store these signals in the form of test files by selecting the **Save Tx Raw Data into a File** option. Note that the play button must be pressed before data is populated in these files.
- User generated data files can be selected using the **Load Tx1** button and the **Load Tx2** button. Format the data files as one I sample and one Q sample per line. Each I or Q sample must be in the range from +32767 to -32768. If the I and Q samples are smaller than this range, the software scale them up to numbers in the correct range. The file size is limited to four mega samples (MS) for each channel (I data = 4 MS maximum, and Q data = 4 MS maximum).

Pressing the play symbol moves the [ADRV9008-2](#) or [ADRV9009](#) to the transmit state and starts a process where the generated CW data or the I/Q data in the Transmitter 2 files are sent to the transceiver. The data is stored on the Zynq motherboard RAM and the RAM pointer loops through the data continuously until the stop button is pressed.

The **Tx2 Attenuation (dB)** input allows the user to control the analog attenuation in the Transmitter 2 channel. This input provides 0.05 dB of attenuation control accuracy. The **Tx1 Attenuation (dB)** input performs the same operation on the Transmitter 1 channel.

The **Tx2 LOL Tracking** tick box enables a transmitter LOL calibration. This calibration improves the LOL performance on the Transmitter 2 channel. The **Tx1 LOL Tracking** tick box performs the same operation on the Transmitter 1 channel. To perform transmitter LOL tracking calibrations, external circuitry is required to route transmitter signals back through an observation receiver input. For more details, refer to the Hardware Setup for External Transmitter LO Leakage Calibration section. Note that, for external transmitter LOL tracking calibration, both transmitters must be looped back to both observation receivers through splitters and attenuators.

The **Tx2 QEC Tracking** tick box enables a transmitter QEC calibration on the Transmitter 2 channel. This calibration improves the QEC performance. The **Tx1 QEC Tracking** tick box performs the same operation on the Transmitter 1 channel.

The **Tx2 Routed to Orx1** tick box advises the software that the user has configured an external loopback path from the Transmitter 2 output to Observation Receiver 1. The **Tx1 Routed to Orx2** tick box performs the same operation for the Transmitter 1 channel.

The **Tx Init External LOL** button runs an external LOL initial calibration.

## TIME DIVISION DUPLEX (TDD) MODE

The ADRV9009 transceiver evaluation hardware, together with TES, provides the capability to demonstrate TDD operation.

### LTE TDD FRAME STRUCTURE

Preset configurations provided in the TES follow 3GPP specifications, in which Frame Structure Type 2 is used for TDD operation. In this configuration, each 10 ms radio frame consists of two 5 ms half frames. Each half frame consists of five 1 ms subframes. The supported uplink and downlink configurations are listed in Table 1, where the following parameters are described for each subframe in a radio frame:

- D denotes which subframe is reserved for downlink transmissions.

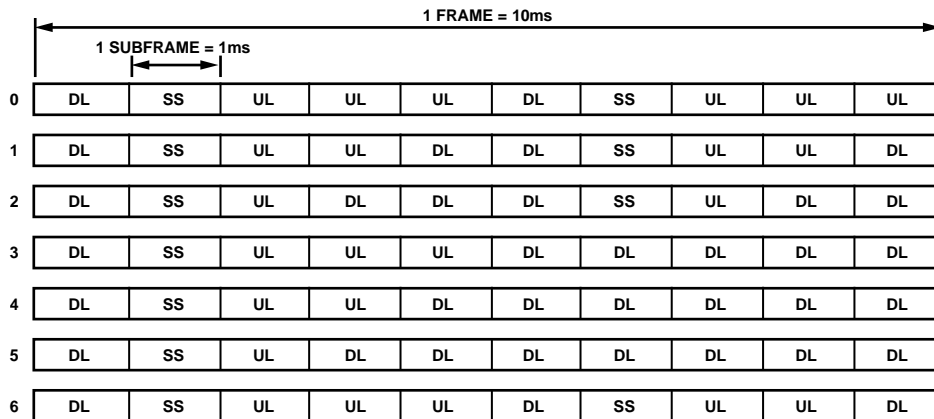
- U denotes which subframe is reserved for uplink transmissions.
- S denotes a special subframe with the following three fields: downlink pilot time slot (DwPTS), guard period (GP), and uplink pilot time slot (UpPTS)

The TES provides preset configurations for all uplink and downlink configurations, with both 5 ms and 10 ms downlink to uplink switch point periodicity. All preset configurations are shown in Figure 38. In the case of a 5 ms downlink to uplink switch point periodicity, the special subframe exists in both half frames. In the case of a 10 ms downlink to uplink switch point periodicity, the special subframe exists in the first half frame only.

Table 1. Uplink and Downlink Configurations

Uplink/Downlink Configuration No.	Downlink/Uplink Switch Point Periodicity (ms)	Subframe Number <sup>1</sup>									
		0	1	2	3	4	5	6	7	8	9
0	5	D	S	U	U	U	D	S	U	U	U
1	5	D	S	U	U	D	D	S	U	U	D
2	5	D	S	U	D	D	D	S	U	D	D
3	10	D	S	U	U	U	D	D	D	D	D
4	10	D	S	U	U	D	D	D	D	D	D
5	10	D	S	U	D	D	D	D	D	D	D
6	5	D	S	U	U	U	D	S	U	U	D

<sup>1</sup> D means a downlink subframe, S means a special switching subframe, and U means an uplink subframe.



DL = DOWNLINK SUBFRAME  
UL = UPLINK SUBFRAME  
SS = SPECIAL SWITCHING SUBFRAME

Figure 38. Graphical Representation of Uplink and Downlink Configurations in the TDD Frame

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## ADRV9009 EVALUATION HARDWARE IN TDD MODE

For TDD operation, the initialization calibrations are run just as they are for FDD mode. After the initialization calibrations are complete, the TDD command is used to place the device in TDD mode. TDD mode works only when configuring the GUI for the ADRV9009 hardware.

The FPGA on the Zynq platform contains a configurable TDD state machine that can be used to control the TX\_ENABLE, RX\_ENABLE, and GPIO signals provided to the transceiver. The **TDD/FDD Switching** tab in the TES allows enabling and disabling of the TDD state machine and configuration of the transmitter and receiver regions in the TDD frame pulse to either a preset LTE TDD configuration, or a user-defined configuration.

The ARM processor inside ADRV9009 uses the RX\_ENABLE, TX\_ENABLE, and GPIO signals controlled by the Zynq FPGA to determine when the device is in the receiver state, transmitter state, observation receiver state, and so on. Figure 39 is a timing diagram of the TX\_ENABLE and RX\_ENABLE signals during the LTE Configuration 0 type frame. The ADRV9009 respond based on the level of the TX\_ENABLE and RX\_ENABLE signals. Note that the minimum duration for RX\_ENABLE or TX\_ENABLE is 500  $\mu$ s for proper calibration operation.

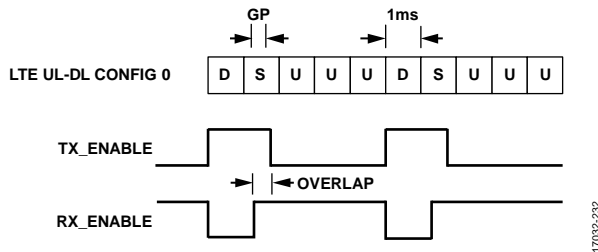


Figure 39. Timing Diagram Showing Example RX\_ENABLE/TX\_ENABLE Signaling for LTE Uplink/Downlink Configuration 0

## SETTING UP TDD FUNCTIONALITY

To operate the ADRV9009 evaluation system and TES in TDD mode, the user must perform the steps described in the following sections.

### Hardware Configuration

Follow the description of hardware configuration in the Hardware Setup section.

The ADRV9009 evaluation system provides a synchronization pulse on the Zynq motherboard SMA connector, J67. The user can use this pulse to synchronize external measurement equipment. Fine tune this signal using the TES interface described in the TES Interface for TDD Mode section. After all hardware is connected properly, the user can start configuring the software.

For successful TDD operation, ensure that the following setup is available:

- TES Version 1.0.25.0 or above
- Dynamic link library (DLL) Version 1.0.29.20 or above
- Command Server Version 1.0.29.20 or above
- FPGA Version 4E000101 or above
- Arm Version 0.07.04 or above
- Stream Version 0.00.01 or above

### TES Configuration

Perform the following procedure before enabling TDD mode using the TES:

1. Using the TES interface described in the Configuring the ADRV9008-2 Transmitter section, select profiles for the receiver channels, transmitter channels, and observation receiver channels as follows:
  - Receiver = 200 MHz, I/Q rate = 245.76 MHz
  - Transmitter = 200 MHz/450 MHz, I/Q rate = 491.52 MHz
  - Observation receiver = 450 MHz, I/Q rate = 491.52 MHz
2. Configure the JESD204B section of the TES as follows (Figure 40 shows a typical setup for JESD204B in the TES):
  - Set the receiver framer selection to Framer A.
  - Set the observation receiver framer selection to Framer B.
  - Set the transmitter deframer selection to either Deframer A or Deframer B.
  - Ensure that the lane rates for Framer A and Observation Receiver Framer B are the same.
  - Ensure that Framer A and Observation Receiver Framer B do not use the same lanes.

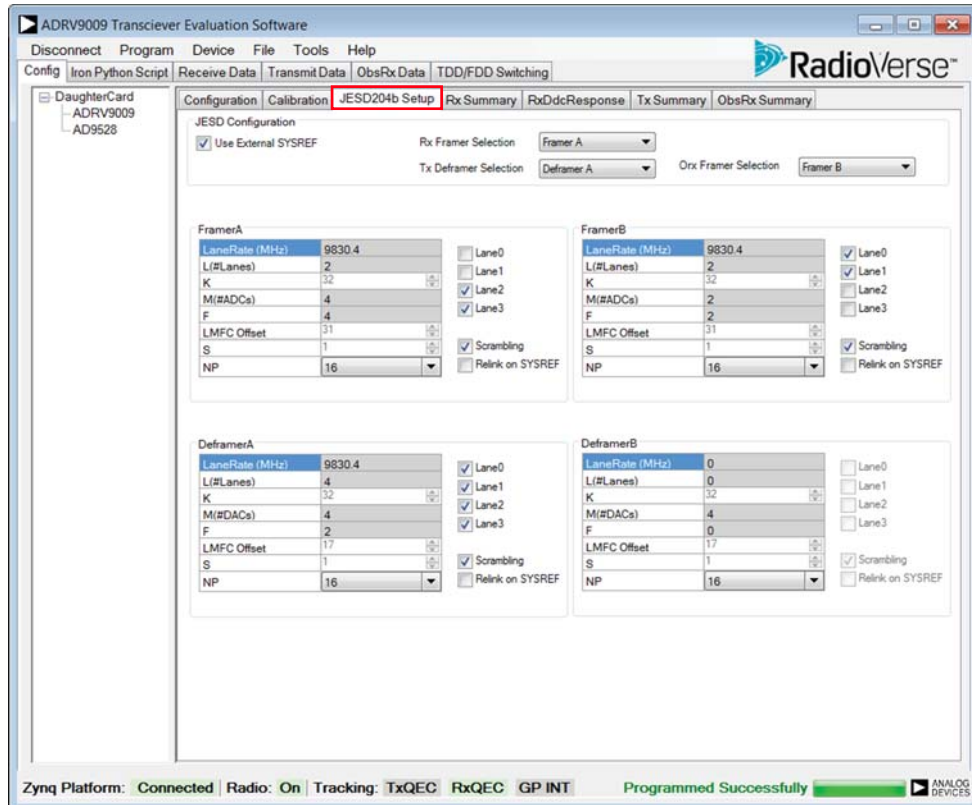


Figure 40. Typical JESD204B Setup for TDD Operation in the TES

3. Using the calibration page described in the Configuring the ADRV9008-2 Transmitter section, enable the desired calibrations.
4. After all configuration is complete, program the ADRV9009 evaluation system by clicking the **Program** button.
5. After the ADRV9009 evaluation system is programmed, move to the **Receiver Data** tab shown in Figure 34. In this tab,
  - a. Set the receiver trigger to TDD\_SM\_PULSE.
  - b. Set the sample time to be at least 1 frame length (10 ms for standard LTE TDD Type 2 frame structures, described in the LTE TDD Frame Structure section).
  - c. Click on play button.
6. Next, click on the **Transmit Data** tab shown in Figure 36. In this tab,
  - a. Load data files that are time aligned with the desired LTE TDD Type 2 frame structure. The TES provides an example data file that can be used with the LTE TDD 0 Type 2 frame structure. For more information, see the TES Interface for TDD Mode section.
  - b. Click the play button.
7. After the ADRV9009 evaluation system is programmed, move to the **ObsRx Data** tab shown in Figure 35. In this tab,
  - a. Set the receiver trigger to TDD\_SM\_PULSE.
  - b. Set the sample time to be at least 1 frame length (10 ms for standard LTE TDD Type 2 frame structures, described in the LTE TDD Frame Structure section).
  - c. Click the play button.
8. The final step requires the user to select the desired TDD timing profile using the **TES TDD/FDD Switching** tab shown in Figure 41. See the TES Interface for TDD Mode section for a detailed description of this tab. After all timing settings are configured,
  - a. Click the **SetUp TDD Timings** button.
  - b. Click the **Enable Tx Data Transmit** button.

If the user does not follow this sequence, the TES software provides real-time pop-up warning messages. These messages inform the user about possible misconfigured settings.

## TES INTERFACE FOR TDD MODE

If the device is programmed successfully, the **TDD/FDD Switching** tab in the TES becomes active. Figure 41 shows the TES TDD interface tab. The parameters available to the user in this tab are as follows:

- Preset** allows the user to select one of seven LTE TDD Type 2 frame structures (see the LTE TDD Frame Structure section) and provides options for user specific TDD frame timing. If the user selects one of seven LTE TDD Type 2 frame structures, then all the following parameters provide detailed timing information for enabling and disabling the RF signal paths. If the user selects custom mode, then all parameters described are allowed to configure the desired RF paths with user specific timing. The TES also provides a special mode called custom LTE TDD0. This mode configures the [ADRV9009](#) hardware and software with LTE TDD 0 frame timing optimized specifically to suit the evaluation platform. The TES also provides transmitter data files with timing optimized for this particular mode. Users can find these files in the **Resources** subfolder, located inside the TES installation folder. The name of the file is **TDD\_491p52MSPS\_20M\_TM3p1\_Cfg0.txt**.
- The **Total Frame Time[us]** field determines the total length of a single TDD frame in microseconds.

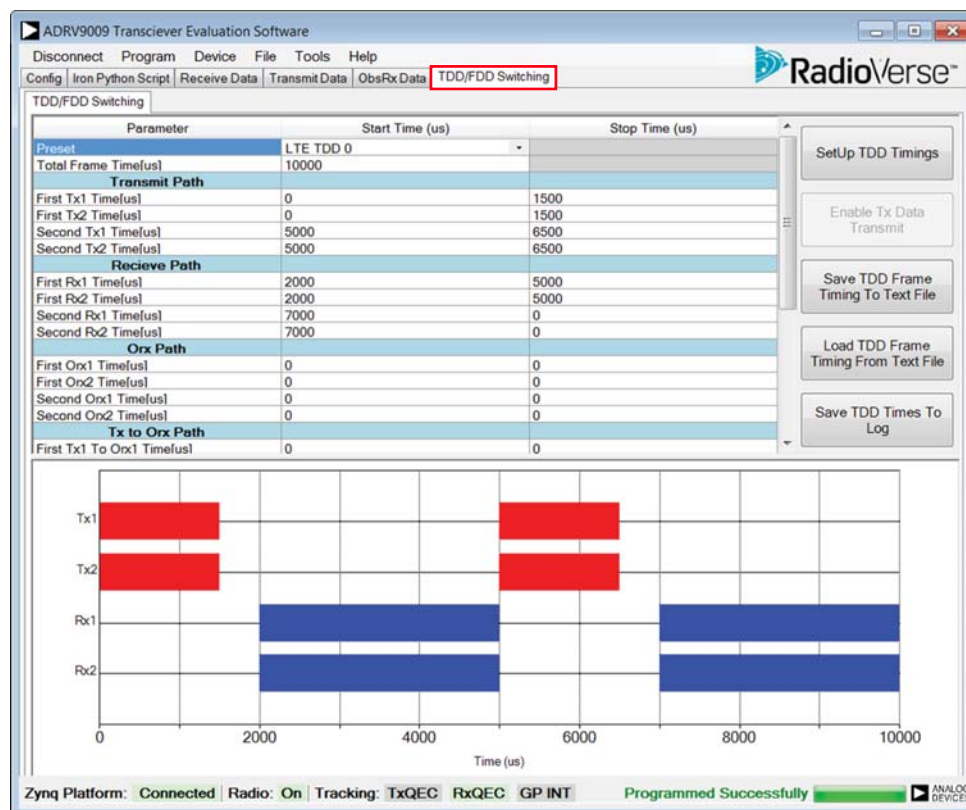


Figure 41. TES TDD Interface Tab

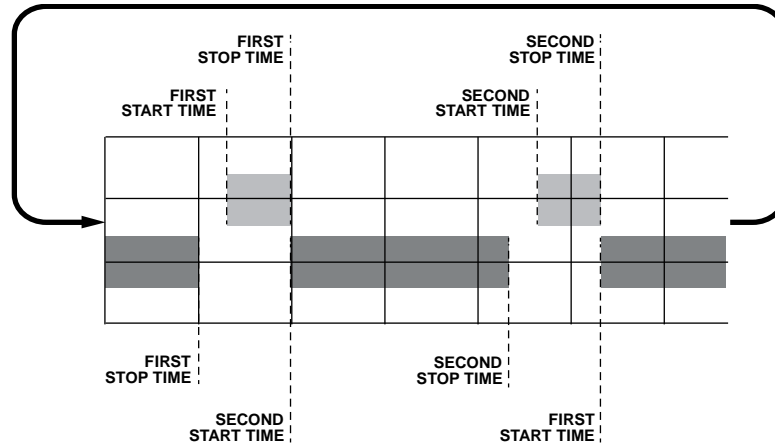


Figure 42. Naming Convention Used for TDD Start/Stop Description in TES

A section of TDD parameters, **Transmit Path**, allows the user to control the following fields:

- The **First Tx2 Time[μs]** field determines the beginning and end of the first Transmitter 2 subframes (or group of subframes). The **Start Time (μs)** column determines the beginning of a subframe (or group of subframes) in a single frame. The **Stop Time (μs)** column determines the end of a subframe (or group of subframes) in a single frame. The TES TDD interface follows the convention where a subframe (or group of subframes) is enabled at the end and at the beginning of a frame border, and then the start is marked at the end of a single frame. Figure 42 provides a graphical explanation of the naming conventions used in the TES.
- The **First Tx2 Time[μs]** field determines the beginning and end of the first Transmitter 2 subframe (or group of subframes).
- If more than one Transmitter 2 subframe (or group of subframes) is used, then the **Second Tx2 Time[μs]** field determines the beginning and end of the second Transmitter 2 subframe (or group of subframes).
- If more than one Transmitter 2 subframe (or group of subframes) is used, then the **Second Tx2 Time[μs]** field determines the beginning and end of the second Transmitter 2 subframe (or group of subframes).

A section of TDD parameters called **Receive Path** allows the user to control the following fields:

- The **First Rx1 Time[μs]** field determines the beginning and end of the first Receiver 1 subframe (or group of subframes).
- The **First Rx2 Time[μs]** field determines the beginning and end of the first Receiver 2 subframe (or group of subframes).
- If more than one Receiver 1 subframe (or group of subframes) is used, then the **Second Rx1 Time[μs]** field determines the beginning and end of the second Receiver 1 subframe (or group of subframes).

- If more than one Receiver 2 subframe (or group of subframes) is used, then the **Second Rx2 Time[μs]** field determines the beginning and end of the second Receiver 2 subframe (or group of subframes).

A section of TDD parameters called **Orx Path** allows the user to control the following fields:

- The **First Orx1 Time[μs]** field determines the beginning and end of the first Observation Receiver 1 subframe (or group of subframes).
- The **First Orx2 Time[μs]** field determines the beginning and end of the first Observation Receiver 2 subframe (or group of subframes).
- If more than one Observation Receiver 1 subframe (or group of subframes) is used, then the **Second Orx1 Time[μs]** field determines the beginning and end of the second Observation Receiver 1 subframe (or group of subframes).
- If more than one Observation Receiver 2 subframe (or group of subframes) is used, then the **Second Orx2 Time[μs]** field determines the beginning and end of the second Observation Receiver 2 subframes (or group of subframes).

A section of TDD parameters called **Tx to Orx Path** allows the user to control external signal routing for external LOL initialization calibrations and tracking calibrations using the following fields:

- The **First Tx2 to Orx1 Time[us]** field determines the beginning and end of the first Transmitter 2 to Observation Receiver 1 subframe (or group of subframes).
- The **First Tx2 to Orx2 Time[us]** field determines the beginning and end of the first Transmitter 2 to Observation Receiver 2 subframe (or group of subframes).

- If more than one Transmitter 2 to Observation Receiver 1 subframe (or group of subframes) is used, then the **Second Tx2 to Orx1 Time[us]** field determines the beginning and end of the second Transmitter 2 to Observation Receiver 1 subframe (or group of subframes).
- If more than one Transmitter 2 to Observation Receiver 2 subframe (or group of subframes) is used, then the **Second Tx2 to Orx2 Time[us]** field determines the beginning and end of the second Transmitter 2 to Observation Receiver 2 subframe (or group of subframes).
- The **First Tx2 to Orx1 Time[us]** field determines the beginning and end of the first Transmitter 2 to Observation Receiver 1 subframe (or group of subframes).
- The **First Tx2 to Orx2 Time[us]** field determines the beginning and end of the first Transmitter 2 to Observation Receiver 2 subframe (or group of subframes).
- If more than one Transmitter 2 to Observation Receiver 1 subframe (or group of subframes) is used, then the **Second Tx2 to Orx1 Time[us]** field determines the beginning and end of the second Transmitter 2 to Observation Receiver 1 subframes (or group of subframes).
- If more than one Transmitter 2 to Observation Receiver 2 subframe (or group of subframes) is used, then the **Second Tx2 to Orx2 Time[us]** field determines the beginning and end of the second Transmitter 2 to Observation Receiver 2 subframe (or group of subframes).

If the user programmed [ADRV9009](#) using Observation Channel 1, then an error message appears if the user attempts to set up the TDD timings and enters values in the **Tx2 to Orx2** field. A further requirement of the observation receiver path assignment relates to the minimum duration of an ARM tracking calibration in any one instance. This duration is 500  $\mu$ s. This requirement is due to the tracking calibrations needing at least 500  $\mu$ s of data to perform a meaningful observation.

The section of TDD parameters named **Misc** allows the user to control the following fields:

- The **Tx Path Delay (+/- $\mu$ s)** field allows the user to delay data sent to the transmitter path over the JESD204B interface in reference to the TX\_ENABLE signal.
- The **Rx Path Delay (+/- $\mu$ s)** field allows the user to delay data received from the receiver path over the JESD204B interface in reference to the RX\_ENABLE signal.
- The **Obs Rx Path Delay (+/- $\mu$ s)** field allows the user to delay data received from the observation receiver path over the JESD204B interface in reference to the ORX\_ENABLE signal.

- In TDD mode, the [ADRV9008-1](#), [ADRV9008-2](#), and [ADRV9009](#) evaluation hardware generates a pulse on SMA Connector J67, located on the Zynq platform. The **External Trigger [ $\mu$ s]** parameter allows the user to control the position and the width of this pulse in reference to the start of the TDD frame.
- The **Loop N Times** option allows user to control the number of loop repetitions. The allowable range is from 1 to 15, or the loop repetition continues until stopped.

The bottom part of the **TDD/FDD Switching** tab in the TES provides a diagram with a graphical representation of the timing parameters entered in the table above. This feature allows the user to visually represent activities on the receiver and transmitter datapaths.

The TDD page also contains four buttons to interact with the user. These buttons include

- **SetUp TDD Timing.** Pressing this button causes the current TDD configuration stop/start parameters from the table to be written into the FPGA and sets up the state machine for operation. This button also zeroes the transmitter datapath, resets the transmitter RAM pointer to the start address of the data, and then reconnects the transmitter RAM to the transmitter datapath. Finally, this button enables the TDD state machine and starts the data. After the evaluation system is in the TDD state, this button changes its name to **Disable TDD**. Pressing this button stops the TDD state machine.
- **Enable Tx Data Transmit.** After the user sets up TDD mode and presses the **SetUp TDD Timing** button, the [ADRV9009](#) evaluation system enables the TDD state machine and TDD mode becomes operational. There is no data present at the transmitter output until the user presses the **Enable Tx Data Transmit** button. This button enables the data transfer in the FPGA. The transmitter datapath is zeroed until the **Enable Tx Data Transmit** button is pressed (data does not start until the **Enable Tx Data Transmit** button is pressed). After entering TDD mode, the transmitter data is sent continuously to the device through the JESD204B link (which is not gated by the TX\_ENABLE signal). Therefore, the TDD transmitter data files must be properly time aligned to the TDD state machine signals.
- The **Save TDD Frame Timing** button allows the user to save a TDD timing to the file in a text readable format.
- The **Load TDD Frame Timing** button allows the user to load TDD timing information from the previously saved TDD timing file.



## SCRIPTING

After the user configures the device to the desired profile, a script can be generated with all API initialization calls in the form of IronPython functions. Use the **Tools > Create Script > Python** button to accomplish this task. This button is located on top of the **Config** tab.

The **Iron Python Script** tab allows the user to use IronPython language to write a unique sequence of events and then execute them using an evaluation system.

Scripts generated using the **Save Python Script** button can be loaded, modified if needed, and run in the **Iron Python Script** tab. Figure 43 shows the **Iron Python Script** tab after executing the new script function. The top part of the window contains IronPython commands, and the bottom part of the window displays the script output.

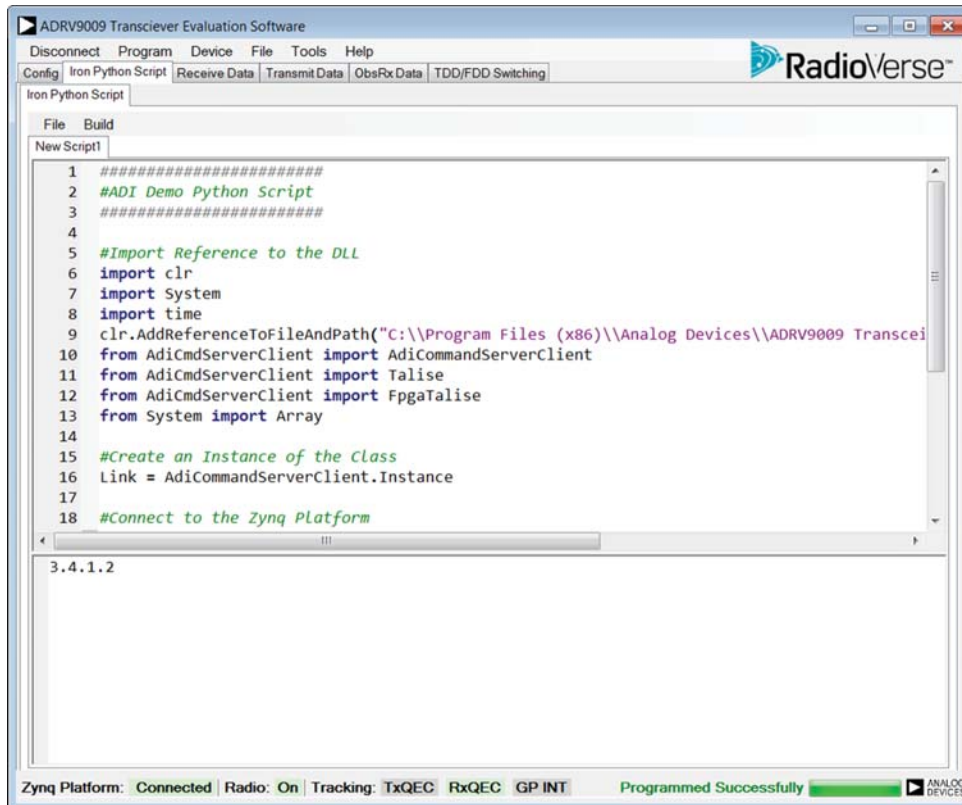


Figure 43. Iron Python Script Tab

### IronPython Script Example

The following example, which is generated after selecting the **New** button in the **Iron Python Script** tab, returns the version of command interpreter software running on the Zynq platform:

```
#Import Reference to the DLL
import clr

clr.AddReferenceToFileAndPath("C:\\Program Files (x86)\\Analog Devices\\ADRV900x Transceiver
Evaluation Software\\AdiCmdServerClient.dll")
from AdiCmdServerClient import AdiCommandServerClient
from AdiCmdServerClient import Talise

#Create an Instance of the Class
Link = AdiCommandServerClient.Instance

#Connect to the Zynq Platform
```



```
if(Link.hw.Connected == 1):  
    Connect = 0  
else:  
    Connect = 1  
    Link.hw.Connect("192.168.1.10", 55555)
```

```
#Read the Version  
print Link.Version()
```

```
#Disconnect from the Zynq Platform  
if(Connect == 1):  
    Link.hw.Disconnect()
```

When using the Iron Python window, the user can execute any API command.

A list of all API commands is provided in the TES in **Help > API Help**. All [ADRV9008-1](#), [ADRV9008-2](#), and [ADRV9009](#) API functions, when called in the **Iron Python** window, must be renamed to reflect the following IronPython mnemonic:

ADRV900X -> Talise.

Add a header with a new class instance for a new connection. For example, after calling

```
#Create an Instance of the Class  
Link = AdiCommandServerClient.Instance
```

the new class instance for the [ADRV9008-1](#), [ADRV9008-2](#), and [ADRV9009](#) evaluation hardware is

```
Link.
```

An example of an API function call using Iron Python is as follows (if the user wants to check the gain index for Receiver 1 using the following [ADRV9008-1](#), [ADRV9008-2](#), and [ADRV9009](#) API function):

```
TALISE_GetRxGain
```

Then, the user calls the IronPython function that follows (assuming the platform is initialized using the example code previously described):

```
print Link.Talise.GetRxGain(Link.Talise.RxChannel.Rx1, 0)
```

For a complete list of available script commands, refer to the **Talise\_TCPIP\_Client\_Library.chm** file located in the **Resources** folder of the TES.

## TROUBLESHOOTING

The following section is a quick help guide describing what to do if the system is not operational. This guide assumes that the user follows the instructions and the hardware configuration described in this user guide.

### STARTUP

#### No LED Activity

If there is no LED activity at startup,

1. Check if the board is properly powered. There must be 12 V present at the J22 input, and after powering the Zynq platform on (SW1 is turned on), the following must be true:
  - The fan on the Zynq platform is activated.
  - A number of green LEDs on the Zynq platform near SW1 are on with no red LEDs active on the Zynq platform.
  - The Zynq GPIO LEDs follow the sequence described in the Hardware Operation section.
2. If the LED sequence does not follow the sequence described, check the jumper settings and the SW11 positions on the Zynq platform. If these settings and positions are correct, check if the SD card is correct and properly inserted in the J30 socket. Use the SD card supplied with the evaluation kit.

If there is still a problem and the user is certain that the Zynq platform is operational, contact an Analog Devices representative for help.

#### LEDs Active, Hardware Not Connected

If the LEDs are active, but the TES reports that the hardware is not connected,

1. Check if the Ethernet cable is properly connected between the PC used to run the TES and the Zynq platform. The LEDs on the Zynq platform next to the Ethernet socket flash when the connection is active.
2. If the cable is properly connected, check if the Windows operating system is able to communicate over the Ethernet port with the Zynq platform. Check if the IP number and the open ports for the Ethernet connection used to communicate with the Zynq platform follow the guidelines described in the Hardware Setup section.
3. Run **cmd.exe** and then type `ping 192.168.1.10`. The can then see a reply from the Zynq platform. If no reply is received, connection with the Zynq platform must be re-examined.
4. If connection with the Zynq platform is established but the TES still reports that hardware is not available, ensure that Port 22 (SSH) and Port 55555 (evaluation software) are not blocked by firewall software on the Ethernet connection used to communicate with the Zynq platform. Both ports are required to be open for normal operation.

### ERROR HANDLING

The TES provides the user a number of error messages in the event of problems with hardware or software configuration. The error messages displayed by the TES are listed in Table 2. For each error, the table contains an explanation of how to interpret the reason for the error message and what action must be performed to solve potential problems.

**Table 2. Error Messages and Possible Solutions**

Error Message	Description
A connection attempt failed because the connected party did not properly respond after a period of time, or established connection failed because connected host failed to respond An established connection was aborted by the software in your host machine	These messages indicate that the user attempted to establish connection before readying the hardware. To solve this problem, perform a power cycle of the Zynq platform and wait until the hardware is fully booted up. The LED indication that system is ready is described in the Hardware Operation section.
Connection was terminated by remote host  An existing connection was forcibly closed by the remote host	These messages are shown when the Ethernet cable is disconnected or when the Zynq board loses power. To resolve this issue, check if all hardware connections are correct, and that the Zynq motherboard and <a href="#">ADRV9008-1</a> , <a href="#">ADRV9008-2</a> , and <a href="#">ADRV9009</a> daughter card are powered. Also, restart the <a href="#">ADRV9008-1</a> , <a href="#">ADRV9008-2</a> , and <a href="#">ADRV9009</a> transceiver evaluation software.
Cannot connect to device	This message is shown when power to the <a href="#">ADRV9008-1</a> , <a href="#">ADRV9008-2</a> , and <a href="#">ADRV9009</a> daughter card is lost. Ensure that <a href="#">ADRV9008-1</a> , <a href="#">ADRV9008-2</a> , and <a href="#">ADRV9009</a> daughter card is connected to J37 on the Zynq board and that the 6 V supply is adequately connected. The Hardware Operation section describes the correct status of the LEDs on the <a href="#">ADRV9008-1</a> , <a href="#">ADRV9008-2</a> , and <a href="#">ADRV9009</a> daughter card.

Error Message	Description
AD9528 REFCLK not detected or PLLs not locked	This message indicates that clock chip is not able to lock to the reference signal. Potential problems in this scenario include a lack of reference signal, incorrect amplitude, or incorrect frequency. Ensure that external reference clock is connected to the J401 SYSREF_IN SMA connector at the <a href="#">ADRV9008-1</a> , <a href="#">ADRV9008-2</a> , and <a href="#">ADRV9009</a> daughter card as shown in Figure 2. The reference frequency must match the frequency selected in the <a href="#">AD9528</a> configuration tab, as shown in Figure 31. The amplitude of the reference signal must not exceed 5 dBm. Correct hardware and software configuration of the reference clock is indicated by the LED status on the <a href="#">ADRV9008-1</a> , <a href="#">ADRV9008-2</a> , and <a href="#">ADRV9009</a> daughter card as described in the Hardware Operation section.
All lane rates are 0 Gbps (disabled)	This message indicates that all the transmitter and receiver paths are disabled. At least one of the paths must be enable when programming the transceiver.
No Rx lanes enabled. Please check selection of Rx lanes	This message is related to the JESD204B interface configuration. If the receiver path is enabled and there are no receiver lanes on the JESD204B interface assigned to the receiver path, then this error message appears. Select the appropriate lanes for the receiver using the TES tab shown in Figure 26. Similarly, this error message is shown for the transmitter or observation receiver JESD204B setup.
Rx lane rate too high. Please check selection of Rx lanes Invalid Tx K value	These messages relate to the JESD204B interface configuration. Ensure that the lane rates for the receiver framer, observation receiver framer, and transmitter deframer match.
Error during ADRV900x RF PLL frequency setup: ERROR:34 setRFPIIFrequency	This message appears when the user uses the external LO frequency, but the frequency is different than expected.
Error during setting of ADRV900x ENSM state: ERROR:5 setEnsmState Synchronization error. Please power cycle TES and Zynq Platform No hardware connection	These messages are generated when system is in invalid state. To resolve the problem please restart the TES and power cycle the Zynq platform.

**ESD Caution**

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

**Legal Terms and Conditions**

By using the evaluation board discussed herein (together with any tools, components documentation or support materials, the "Evaluation Board"), you are agreeing to be bound by the terms and conditions set forth below ("Agreement") unless you have purchased the Evaluation Board, in which case the Analog Devices Standard Terms and Conditions of Sale shall govern. Do not use the Evaluation Board until you have read and agreed to the Agreement. Your use of the Evaluation Board shall signify your acceptance of the Agreement. This Agreement is made by and between you ("Customer") and Analog Devices, Inc. ("ADI"), with its principal place of business at One Technology Way, Norwood, MA 02062, USA. Subject to the terms and conditions of the Agreement, ADI hereby grants to Customer a free, limited, personal, temporary, non-exclusive, non-sublicensable, non-transferable license to use the Evaluation Board FOR EVALUATION PURPOSES ONLY. Customer understands and agrees that the Evaluation Board is provided for the sole and exclusive purpose referenced above, and agrees not to use the Evaluation Board for any other purpose. Furthermore, the license granted is expressly made subject to the following additional limitations: Customer shall not (i) rent, lease, display, sell, transfer, assign, sublicense, or distribute the Evaluation Board; and (ii) permit any Third Party to access the Evaluation Board. As used herein, the term "Third Party" includes any entity other than ADI, Customer, their employees, affiliates and in-house consultants. The Evaluation Board is NOT sold to Customer; all rights not expressly granted herein, including ownership of the Evaluation Board, are reserved by ADI. CONFIDENTIALITY. This Agreement and the Evaluation Board shall all be considered the confidential and proprietary information of ADI. Customer may not disclose or transfer any portion of the Evaluation Board to any other party for any reason. Upon discontinuation of use of the Evaluation Board or termination of this Agreement, Customer agrees to promptly return the Evaluation Board to ADI. ADDITIONAL RESTRICTIONS. Customer may not disassemble, decompile or reverse engineer chips on the Evaluation Board. Customer shall inform ADI of any occurred damages or any modifications or alterations it makes to the Evaluation Board, including but not limited to soldering or any other activity that affects the material content of the Evaluation Board. Modifications to the Evaluation Board must comply with applicable law, including but not limited to the RoHS Directive. TERMINATION. ADI may terminate this Agreement at any time upon giving written notice to Customer. Customer agrees to return to ADI the Evaluation Board at that time. LIMITATION OF LIABILITY. THE EVALUATION BOARD PROVIDED HEREUNDER IS PROVIDED "AS IS" AND ADI MAKES NO WARRANTIES OR REPRESENTATIONS OF ANY KIND WITH RESPECT TO IT. ADI SPECIFICALLY DISCLAIMS ANY REPRESENTATIONS, ENDORSEMENTS, GUARANTEES, OR WARRANTIES, EXPRESS OR IMPLIED, RELATED TO THE EVALUATION BOARD INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, TITLE, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS. IN NO EVENT WILL ADI AND ITS LICENSORS BE LIABLE FOR ANY INCIDENTAL, SPECIAL, INDIRECT, OR CONSEQUENTIAL DAMAGES RESULTING FROM CUSTOMER'S POSSESSION OR USE OF THE EVALUATION BOARD, INCLUDING BUT NOT LIMITED TO LOST PROFITS, DELAY COSTS, LABOR COSTS OR LOSS OF GOODWILL. ADI'S TOTAL LIABILITY FROM ANY AND ALL CAUSES SHALL BE LIMITED TO THE AMOUNT OF ONE HUNDRED US DOLLARS (\$100.00). EXPORT. Customer agrees that it will not directly or indirectly export the Evaluation Board to another country, and that it will comply with all applicable United States federal laws and regulations relating to exports. GOVERNING LAW. This Agreement shall be governed by and construed in accordance with the substantive laws of the Commonwealth of Massachusetts (excluding conflict of law rules). Any legal action regarding this Agreement will be heard in the state or federal courts having jurisdiction in Suffolk County, Massachusetts, and Customer hereby submits to the personal jurisdiction and venue of such courts. The United Nations Convention on Contracts for the International Sale of Goods shall not apply to this Agreement and is expressly disclaimed.

